

Description

[0001] The present invention relates to a solid-state imaging device and to a method for manufacturing the solid-state imaging device, and more particularly, to a solid-state imaging device of chip-sized packed (CSP) having a microlens integrated on a chip.

[0002] Demand for a more compact solid-state imaging element including a CCD (Charge-Coupled Device) is growing, for reasons of a necessity for application of the solid-state imaging element to portable cellular phones and digital cameras.

[0003] A solid-state imaging device, in which microlenses are provided in respective light-receiving regions of a semiconductor chip, has been proposed as one type of solid-state imaging element. Among solid-state imaging devices, a solid-state imaging device has been proposed in JP-A-7-202152, wherein the solid-state imaging device is packaged integrally such that an airtight sealing section is formed between each of the light-receiving regions and the corresponding microlens, thereby making an attempt to miniaturize the solid-state imaging device.

[0004] Such a configuration enables a reduction in footprint and bonding of optical components, such as a filter, a lens, and a prism, on the surface of an airtight sealing section. As a result, an attempt can be made to reduce a packaging size without involvement of a reduction in the light-gathering power of the microlens.

[0005] However, at the time of mounting of such a solid-state imaging device, the solid-state imaging device is mounted on a support substrate, and an attempt must be made to establish electrical connections by means of a method, such as bonding, to enable extraction of signals to the outside, and seal the solid-state imaging device. This involves a large number of man-hours, which raises a problem of mounting requiring consumption of much time.

[0006] To this end, the present inventors have proposed a method comprising the steps of: forming a plurality of solid-state imaging elements on the surface of a semiconductor substrate; cementing a light-transmission member on the surface of the semiconductor substrate such that gaps are formed so as to oppose respective light-receiving regions of the solid-state imaging element; forming external connection terminals in correspondence with the solid-state imaging elements; and separating bonded elements formed on the external connection terminals for each solid-state imaging element.

[0007] As a result, there is formed a compact solid-state imaging element, wherein a light-transmission member is caused to adhere such that gaps are formed so as to oppose the light-receiving region of the solid-state imaging element.

[0008] However, in relation to such a solid-state imaging element, as miniaturization proceeds, a problem of image noise attributable to the influence of α rays becomes more serious.

[0009] The present invention has been conceived in light of the circumstances and aims at providing a highly reliable solid-state imaging device having high picture quality, by means of lessening the influence of α rays and image noise.

[0010] The present invention also aims at readily providing a highly reliable solid-state imaging device.

[0011] Accordingly, the present invention provides a solid-state imaging device, comprising: a semiconductor substrate having a first surface; a solid-state imaging element in the first surface of semiconductor substrate, the solid-state imaging element comprising a light-receiving region; a light-transmission member having a second surface and a third surface, the second surface being opposite to the third surface, wherein the light-transmission member and the first surface of the semiconductor substrate define a gap between the second surface of the light-transmission member and an outer surface of the light-receiving region (that is, the first surface of the semiconductor substrate are spaced apart so as to define a gap between the second surface of the light-transmission member and an outer surface of the light-receiving region); and an external connection terminal connected to the solid-state imaging element, wherein the light-transmission member comprises low α -ray glass.

[0012] Preferably the light-transmission member has an α -ray threshold limit value of 0.002 or less (DPH/cm²).

[0013] This configuration enables a reduction in the amount of α rays reaching the light-receiving section, thereby reducing the image noise.

[0014] Preferably the solid-state imaging device further comprises a spacer between the second surface of the light-transmission member and the first surface of the semiconductor substrate so that a distance between the outer surface of the light-receiving region and the third surface of the light-transmission member is set to be a predetermined value.

[0015] By means of this configuration, highly accurate positioning can be performed readily by means of interposing the spacers between the solid-state imaging element substrate and the light-transmission member. Preferably the distance between the outer surface of the light-receiving region and the third surface of the light-transmission member is 0.5 mm or more.

[0016] By means of this configuration, even when an imperfection, such as a piece of debris measuring 20 μ m or thereabouts, is present in the surface of the light-transmission member, the density of a shadow projected on the solid-state imaging element can be reduced to such an extent that no adverse effect is particularly exerted on the imaging characteristic.

[0017] Preferably the distance between the outer surface of the light-receiving region and the third surface of the

light-transmission member does not exceed 1.5 mm.

[0018] By means of this configuration, even when a piece of debris which is too small to be visually observed is present, a chance of occurrence of image noise can be prevented. Further, in consideration of a problem related to the size of the device and strength of the device, by means of setting the distance from the light-receiving surface to the surface of the light-transmission member to 1.5mm or less, solid-state imaging elements can be mounted without involvement of deterioration of productivity of the dicing process even when the elements are mounted on a wafer scale.

[0019] Preferably, the spacer comprises silicon.

[0020] According to this configuration, the spacer is analogous to the solid-state imaging element in terms of a coefficient of thermal expansion and hence is superior in workability.

[0021] The spacer can be connected to at least one of the first surface of the semiconductor substrate and the second surface of the light-transmission member via a temperature-curing type adhesive.

[0022] The spacer can also be connected to at least one of the first surface of the semiconductor substrate and the second surface of the light-transmission member via a photo-curing type adhesive.

[0023] When low α -ray glass serving as a light-transmission member is used, the low α -ray glass differs from silicon to be used for forming the solid-state imaging element substrate in terms of thermal expansion coefficient. Hence, warpage arises in the wafer during a heating process required to bond the wafer. Thermal stress is exerted on the solid-state imaging element, and hence a drop arises in reliability or a failure to fix the wafer during subsequent processes is likely to arise. However, the solid-state imaging elements can be manufactured without undergoing a high-temperature process through use of a room temperature-curing type adhesive or a photo-curing type adhesive of, thereby diminishing occurrence of warpage.

[0024] Preferably the width of the spacer is 100 to 500 μm .

[0025] By means of this configuration, a superior sealing characteristic is achieved, and there can be formed small solid-state imaging devices with superior layout (i.e., the number of elements to be fabricated in a single wafer). If the width of the spacer is smaller than 100 μm , sealing may become insufficient or a strength failure may arise. Further, if the width of the spacer exceeds 500 μm , the number of elements to be fabricated in a single wafer is reduced, which in turn raises a problem of a failure to miniaturize the solid-state imaging devices.

[0026] Viewed from a further aspect, the present invention provides a method for manufacturing a solid-state imaging device, comprising the steps of: forming a plurality of solid-state imaging elements in a surface of a semiconductor substrate, each of the solid-state imaging elements comprising a light-receiving region; connecting a light-transmission member that comprises low α -ray glass to the surface of the semiconductor substrate, so as to define a gap between the light-transmission member and an outer surface of the light-receiving region, to form an integrated (connected) member; forming external connection terminals corresponding to the solid-state imaging elements (i.e., forming a plurality of external connection terminals, each of the external connection terminals connecting to each of the solid-state imaging elements), to form an integrated member with the external connection terminals; and separating the integrated member with the external connection terminals, for each of the solid-state imaging elements.

[0027] By means of this configuration, the low α -ray glass is used as the light-transmission member. Solid-state imaging elements are positioned on the wafer scale and mounted in a collective manner, whereby the solid-state imaging elements are integrated. The wafer is then separated on a per-solid-state-imaging-element basis. Hence, a solid-state imaging device which is easy to manufacture, lessens image noise, and has high reliability can be formed.

[0028] More preferably, in the step of connecting the light-transmission member, the light-transmission substrate having indentation sections corresponding to the region where the solid-state imaging elements are formed is prepared, and the light-transmission substrate is connected to the surface of the semiconductor substrate.

[0029] By means of this configuration, the indentation sections can be formed such that gaps are readily provided so as to oppose the respective light-receiving regions, by means of forming the indentation sections in the light-transmission substrate. Hence, the number of components is small, and manufacturing operation is easy.

[0030] Desirably, a process for forming protruding sections by means of selectively removing the surface of the semiconductor substrate so as to enclose the light-receiving regions is provided before the connecting process, and gaps are formed between the light-receiving region and the light-transmission member by means of the protruding sections.

[0031] By means of this configuration, a highly reliable solid-state imaging device can be readily provided with high reliability by means of mounting elements between the respective pairs of protruding sections (spacers) previously formed on the surface of the semiconductor substrate.

[0032] The connecting step is characterized in that a gap is defined between the semiconductor substrate and the light-transmission member by way of the spacers disposed around the light-receiving region.

[0033] Preferably, the connecting step is performed at a temperature which does not exceed 80°C.

[0034] More preferably, the connecting step is a step using a room temperature curing type adhesive.

[0035] Preferably the connecting step is a step using a photo-curing type adhesive.

[0036] By means of such a configuration, the chance of occurrence of warpage in members after bonding can be

reduced even when the members differ from each other in terms of a thermal expansion coefficient.

[0037] Desirably, the connecting step is characterized by using a room temperature-curing type adhesive.

[0038] By means of this configuration, connecting can be effected without increasing a connecting temperature, thereby preventing occurrence of warpage.

[0039] The connecting step can be effected by using a photo-curing type adhesive.

[0040] This configuration also enables connecting without increasing a connecting temperature, thereby preventing occurrence of warpage.

[0041] Further, as a result of a semi-curing type adhesive being used as an adhesive, positioning becomes easy, and more highly accurate position becomes possible.

[0042] Desirably, the method includes a process for sealing the neighborhood of a junction between the light-transmission member and the surface of the semiconductor substrate with resin such that the external connection section is exposed.

[0043] By means of this configuration, intrusion of moisture is suppressed, and a highly reliable solid-state imaging element can be formed.

[0044] Processing pertaining to the resin-sealing process is preferably performed at a temperature which does not exceed 80°C.

[0045] By means of this configuration, connecting can be performed without increasing the connecting temperature, thereby reducing occurrence of warpage.

[0046] Preferred embodiments of the present invention shall now be described by way of example only, with reference to the accompanying drawings, in which:

Fig. 1A is a cross-sectional profile of a solid-state imaging device fabricated according to a method of a first embodiment of the present invention;

Fig. 1B is an enlarged cross-sectional profile of the principal features of the solid-state imaging device;

Figs. 2A to 2D are views showing processes for manufacturing the solid-state imaging device according to the first embodiment of the present invention;

Figs. 3A to 3C are views showing processes for manufacturing the solid-state imaging device according to the first embodiment of the present invention;

Figs. 4A to 4D are views showing processes for manufacturing a solid-state imaging device according to a second embodiment of the present invention;

Figs. 5A to 5E are views showing processes for manufacturing a solid-state imaging device according to a third embodiment of the present invention;

Figs. 6A to 6D are views showing processes for manufacturing a solid-state imaging device according to a fourth embodiment of the present invention;

Figs. 7A to 7D are views showing processes for manufacturing a solid-state imaging device according to a fifth embodiment of the present invention;

Figs. 8A to 8D are views showing processes for manufacturing a solid-state imaging device according to a sixth embodiment of the present invention;

Figs. 9A to 9E are views showing processes for manufacturing a solid-state imaging device according to a seventh embodiment of the present invention;

Figs. 10A to 10D are views showing processes for manufacturing a solid-state imaging device according to an eighth embodiment of the present invention;

Figs. 11A to 11D are views showing processes for manufacturing a solid-state imaging device according to a ninth embodiment of the present invention;

Figs. 12A and 12B are views showing processes for manufacturing a solid-state imaging device according to a tenth embodiment of the present invention;

Fig. 13 is a view showing processes for manufacturing the solid-state imaging device according to the tenth embodiment of the present invention;

Figs. 14A and 14B are views showing processes for manufacturing a solid-state imaging device according to an eleventh embodiment of the present invention;

Figs. 15A to 15C are views showing processes for manufacturing a solid-state imaging device according to a twelfth embodiment of the present invention;

Figs. 16A to 16D are views showing processes for manufacturing a solid-state imaging device according to a thirteenth embodiment of the present invention;

Figs. 17A to 17C are views showing processes for manufacturing a solid-state imaging device according to a fourteenth embodiment of the present invention;

Fig. 18 is a view showing processes for manufacturing a solid-state imaging device according to a fifteenth embodiment of the present invention;

Figs. 19A to 19D are views showing processes for manufacturing a solid-state imaging device according to a sixteenth embodiment of the present invention;

Figs. 20A to 20C are views showing processes for manufacturing a solid-state imaging device according to a seventeenth embodiment of the present invention;

Figs. 21A to 21F are views showing processes for manufacturing a solid-state imaging device according to an eighteenth embodiment of the present invention;

Figs. 22A to 22C are views showing processes for manufacturing a solid-state imaging device according to a nineteenth embodiment of the present invention;

Figs. 23A to 23D are views showing processes for manufacturing a solid-state imaging device according to a twentieth embodiment of the present invention;

Fig. 24 is a view showing processes for manufacturing a solid-state imaging device according to a twenty-first embodiment of the present invention;

Figs. 25A to 25E are views showing processes for manufacturing a solid-state imaging device according to the twenty-first embodiment of the present invention;

Fig. 26 is a view showing processes for manufacturing a solid-state imaging device according to a twenty-second embodiment of the present invention;

Figs. 27A to 27C are views showing processes for manufacturing a solid-state imaging device according to a twenty-third embodiment of the present invention;

Figs. 28A to 28D are views showing processes for manufacturing a solid-state imaging device according to the twenty-third embodiment of the present invention;

Figs. 29A to 29E are views showing processes for manufacturing a solid-state imaging device according to a twenty-fourth embodiment of the present invention;

Figs. 30A and 30B are views showing processes for manufacturing a solid-state imaging device according to a twenty-fifth embodiment of the present invention;

Fig. 31 is a view showing processes for manufacturing a solid-state imaging device according to a twenty-sixth embodiment of the present invention;

Fig. 32 is a view showing processes for manufacturing a solid-state imaging device according to a twenty-seventh embodiment of the present invention;

Fig. 33 is a view showing processes for manufacturing a solid-state imaging device according to a twenty-eighth embodiment of the present invention;

Figs. 34A to 34E are views showing processes for manufacturing the solid-state imaging device according to the twenty-eighth embodiment of the present invention;

Figs. 35A to 35E are views showing processes for manufacturing the solid-state imaging device according to the twenty-fourth embodiment of the present invention;

Figs. 36A to 36C are views showing processes for manufacturing a solid-state imaging device according to a twenty-ninth embodiment of the present invention;

Figs. 37A to 37C are views showing processes for manufacturing a solid-state imaging device according to a thirtieth embodiment of the present invention;

Figs. 38A to 38E are views showing processes for manufacturing a solid-state imaging device according to a thirty-first embodiment of the present invention;

Figs. 39A to 39F are views showing processes for manufacturing a solid-state imaging device according to a thirty-second embodiment of the present invention;

Figs. 40A to 40D are views showing processes for manufacturing a solid-state imaging device according to a thirty-third embodiment of the present invention;

Fig. 41 is a view showing processes for manufacturing a solid-state imaging device according to a thirty-fourth embodiment of the present invention;

Figs. 42A to 42D are views showing processes for manufacturing the solid-state imaging device according to the thirty-fourth embodiment of the present invention;

Figs. 43A to 43C are views showing processes for manufacturing a solid-state imaging device according to the thirty-fourth embodiment of the present invention;

Figs. 44A and 44B are views showing processes for manufacturing a solid-state imaging device according to a thirty-fifth embodiment of the present invention;

Figs. 45A and 45B are views showing processes for manufacturing a solid-state imaging device according to a thirty-sixth embodiment of the present invention;

Figs. 46A to 46D are views showing processes for manufacturing the solid-state imaging device according to the thirty-seventh embodiment of the present invention;

Figs. 47A to 47D are views showing processes for manufacturing a solid-state imaging device according to a thirty-eighth embodiment of the present invention;

Figs. 48A to 48D are views showing processes for manufacturing a solid-state imaging device according to a thirty-ninth embodiment of the present invention;

Fig. 49 is a view showing processes for manufacturing a solid-state imaging device according to a fortieth embodiment of the present invention;

Fig. 50 is a view showing processes for manufacturing a solid-state imaging device according to a forty-first embodiment of the present invention;

Fig. 51 is a view showing the geometry of a sump employed in the embodiments of the present invention; and

Fig. 52 is a view showing a modification of the solid-state imaging element according to the embodiments of the present invention.

[0047] Embodiments of the present invention will be described hereinbelow by reference to the drawings.

(First Embodiment)

[0048] Fig. 1A is a cross-sectional view of a solid-state imaging device, and Fig. 1B is an enlarged cross-sectional view of the principal section of the solid-state imaging device. As shown in Figs. 1A and 1B, sealing cover glass 200 made from low- α -ray glass (CG-1, registered trademark) is formed on the surface of a solid-state imaging element substrate 100 by way of a spacer 203S such that a gap C corresponding to a light-receiving region is created. Glass used as the sealing cover glass has a thickness of 0.5 mm and a refractive index of 1.5. Specifically, a glass substrate 201 serving as a light-transmission member which constitutes the sealing cover glass 200 is cemented to the surface of the solid-state imaging element substrate 100 formed from a silicon substrate 101, the silicon substrate acting as a semiconductor substrate having a solid-state imaging element 102 formed thereon, by way of the spacer 203S such that the gap C is created so as to correspond to the light-receiving region of the silicon substrate 101. The height of the gap C that is, a distance from an outer surface 102a of the light-receiving region to a lower surface of the sealing cover glass; i.e., a surface 201b (a second surface) of the sealing cover glass facing the light-receiving region is set to 0.1 mm or thereabouts. A distance from the outer surface 102a of the light-receiving region to an upper surface of the sealing cover glass; i.e., an outer surface 201a (a third surface) of the sealing cover glass, is set to 0.6 mm or thereabouts. The solid-state imaging device is constituted as follows: Namely, the glass substrate is bonded (connected) to a wafer so as to mount a plurality of elements in a collective manner. Subsequently, the outer edge of the silicon substrate 101 is separated in a piecemeal fashion by means of dicing. Electrical connection with an external circuit (not shown) is achieved by way of bonding pads BP formed on the surface of an outer edge of the silicon substrate 101 exposed from the glass substrate 201. Here, the spacer S203S is set to a height (or thickness) of 10 to 500 μm , preferably 80 to 120 μm . The width α of the spacer is set to 100 to 150 μm or thereabouts.

[0049] As can be seen from the enlarged cross-sectional view of the principal section shown in Fig. 1B, solid-state imaging elements are arranged on the surface of the solid-state imaging element substrate, and the solid-state imaging element substrate is constituted of the silicon substrate 101 having an RGB color filter (filter layer) 46 and microlenses 50 formed thereon.

[0050] The solid-state imaging element is formed such that channel stoppers 28 are formed in a p-well 101b formed on the surface of an n-type silicon substrate 101a and such that a photodiode 14 and a charge transfer element (a vertical charge transfer device (VCCD)) 33 are formed with the respective channel stoppers being sandwiched therebetween. Here, an n-type impurity region 14b is formed within the p-well 101b, to thus form the photodiode 14. Further, a vertical charge transfer channel 20 made from an n-type impurity region having a depth of about 0.3 μm is formed within the p+ channel region 14a. A vertical charge transfer electrode 32 is formed from a polycrystalline silicon layer on the vertical charge transfer channel 20 by way of a gate insulation film 30 made from a silicon oxide film, thereby constituting a charge transfer element 33. A read gate channel 26 is formed from a p-type impurity region between the charge transfer element 33 and the photodiode 14 which reads a signal charge to the vertical charge transfer channel 20.

[0051] The n-type impurity regions 14b remain exposed on the surface 101C (a first surface) of the silicon substrate 101 along the read gate channel 26. After having been temporarily stored in the n-type impurity region 14b, the signal charge developing in the photodiode 14 is read by way of the read gate channel 26.

[0052] The channel stopper 28, which is made from a p+-type impurity region, is present between the vertical charge transfer electrode 32 and the photodiode 14. By means of this channel stopper, the photodiode 14 is electrically isolated from the vertical charge transfer channel 20, as well as from the remaining vertical charge transfer channels 20, so that the vertical charge transfer channels 20 do not come into contact with each other.

[0053] Further, the vertical charge transfer electrode 32 is formed so as to cover the read gate channel 26 and such that the n-type impurity regions 14b become exposed and such that portions of the channel stoppers 28 become exposed. A signal charge is transferred to the vertical charge transfer electrode 32 from the read gate channel 26, to which a read signal is applied and which is located below the vertical charge transfer electrode 32.

[0054] The vertical charge transfer electrode 32 constitutes, along with the vertical charge transfer channel 20, a vertical charge transfer device (VCCD) 33 for vertically transferring a signal charge developing in a p-n junction of the photodiode 14. The surface of the substrate having the vertical charge transfer electrode 32 formed therein is coated with a surface protective film 36, and a light-shielding film 38 made from tungsten is formed on the surface protective film 36. Only a light-receiving region 40 of the photodiode is opened, and the other region is shielded from light.

[0055] The layers provided on the vertical charge transfer electrodes 32 are covered with a planarized insulation film 43 for planarizing a surface and a light-transmission resin film 44 to be formed thereon. The filler layer 46 is formed on the light-transmission resin film 44. In the filter layer 46, a red filter layer 46R, a green filter layer 46G, and a blue filter layer 46B are sequentially arranged in correspondence with the respective photodiodes 14 so as to constitute a predetermined pattern.

[0056] This filter layer 46 is further covered with a microlens array by way of a planarized insulation film 48. This microlens array is constituted of the microlenses 50 which are formed by means of: patterning light-transmission resin including photosensitive resin having a refractive index of 1.3 to 2.0, by means of an etching method using the photolithography; fusing the thus-patterned light-transmission resin and rendering the resin round by means of surface tension; and cooling the thus-rounded resin.

[0057] Processes for manufacturing this solid-state imaging device will now be described. Figs. 2A to 2D and Figs. 3A to 3C are manufacturing process drawings of the processes. As can be seen from the drawings, the processes are based on a so-called wafer-scale CSP method, wherein positioning is performed on a wafer scale; elements are packaged in a collective manner, thereby integrating the elements; and the wafer is separated into solid-state imaging elements. This method is characterized by use of a sealing glass cover 200 with a spacer, for which a spacer 203S has been formed in advance. Here, the drawings show a single unit, but in reality a plurality of solid-state imaging elements are formed.

[0058] Formation of the glass substrate with a spacer will first be described.

[0059] As shown in Fig. 2A, a silicon substrate 203, which is to become a spacer, is caused to adhere to the surface of the glass substrate 201 by way of an adhesive layer 202 formed from an UV-radiation curing adhesive (a cationic polymerizing energy curing adhesive). Here, the glass substrate 201 is made of so-called α -ray glass (CG1; registered trademark), which blocks to a small level an α -ray, which is responsible for image noise. A material containing a small amount of substances which will become α -ray radiation nuclei is desirably used for the glass substrate 201. Moreover, an α -ray limit value is preferably set to 0.002 or less (DPH/cm²). If air bubbles are mixed into the adhesive layer 202, the air bubbles may sometimes cause image noise. Here, the adhesive layer 202 desirably has a thickness of 5 μ m or less. When the thickness is 5 μ m or less, air bubbles having a thickness of 5 μ m or more cannot be present. For this reason, if the distance from the light-receiving surface to a lower surface of the glass substrate is set to 0.08 mm or more, as mentioned previously, occurrence of image noise can be prevented.

[0060] As shown in Fig. 2B, the silicon substrate 203 is etched by means of the etching technique using photolithography while a resist pattern is left in areas which are to become spacers, to thus form the spacers 203S.

[0061] Subsequently, as shown in Fig. 2C, resist is charged into an area between the spacers 203S with exclusion of areas defined between elements while the resist patterns to be used for the spacers 203S remain left, and the glass substrate is etched to a predetermined depth. As a result, as shown in Fig. 2D, an inter-element trench section 204 is formed.

[0062] Here, the width of the spacer is preferably set to 100 to 500 μ m or thereabouts. If the width is smaller than 100 μ m, sealing may become insufficient, or the spacer may become prone to strength failure. Moreover, if the width exceeds 500 μ m or more, the number of elements to be fabricated in a single wafer will be reduced, and there will arise a problem of a failure to miniaturize the solid-state imaging element. Moreover, the distance between the light-receiving surface and the spacer is preferably set to 50 μ m or more, in consideration of seepage of the adhesive.

[0063] Here, the spacer is formed from a silicon substrate. Hence, if etching is effected under conditions that an etch rate of silicon oxide, which is a principal ingredient of the glass substrate, becomes sufficiently faster than the etch rate of silicon, etching can be performed while side walls of the spacer become exposed in the area between the elements. At the time of formation of the inter-element trench section 204, a dicing blade (grindstone) may be employed.

[0064] The only requirement at the time of etching of the spacer is to select etching conditions such that the size of adhering extraneous matters becomes 5 μ m or less. If the adhering extraneous matters measure 5 μ m or less, occurrence of image noise can be prevented, so long as the distance from the light-receiving surface to the lower surface of the glass substrate is set to 0.08 mm or more.

[0065] An adhesive layer 207 of room-temperature curing type is formed on the surfaces of the spacers.

[0066] Photolithography may be performed again, to thus form a resist pattern which covers the entire sidewalls of the spacers. The substrate may be subjected to etching by way of the resist pattern, to thus form the trench sections 204. There is obtained the sealing cover glass 200, in which the trench sections 204 and the spacers 203S are formed in the manner mentioned previously.

[0067] In order to prevent occurrence of the image noise, the height of the spacer is desirably set to 0.08 mm or

more. Moreover, in order to enhance the productivity of the spacer, the height is desirably set to 0.12 mm or less. When the spacers 203S are formed by means of etching, etching may be performed through use of C_4F_8 plasma while the sidewalls of the spacers are protected. Furthermore, a bottom surface may be etched by means of anisotropic etching using SF_6+O_2 plasma.

[0068] Next, the solid-state imaging element substrate is formed. As shown in Fig. 3A, at the time of formation of the element substrate, the silicon substrate 101 (a 6-inch wafer is employed herein) is prepared beforehand, and slice grooves 104 are formed in areas corresponding to separation lines, which are to be used for separating solid-state imaging elements, on the surface of the silicon substrate 101, by means of a method such as etching. Formation of a channel stopper layer, formation of channel regions, and formation of element regions, such as charge transfer electrodes, are performed through use of ordinary silicon processes. A wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0069] Subsequently, as shown in Fig. 3B, positioning is performed by means of alignment marks formed in the outer edge of each substrate, and the sealing cover glass 200 is placed on the solid-state imaging element substrate 100 having the element regions formed therein, in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. Processing pertaining to this process is desirably carried out within a vacuum or an inactive gas atmosphere such as a nitrogen gas. At the time of integration there may be used, a thermosetting adhesive having a thermosetting temperature of 80°C or less, a photo-curing adhesive, which will be described later, or a room-temperature curing adhesive. When the surface of the solid-state imaging element is Si or metal, bonding (connecting) may be achieved by means of surface activation room temperature bonding without use of an adhesive.

[0070] Subsequently, the back of the glass substrate is subjected to CMP (chemical-mechanical polishing), thereby removing the back of the glass substrate 201 to the trench section 204.

[0071] By means of this process, the wafer can be separated into solid-state imaging elements simultaneously with slimming down of the glass substrate. Further, as shown in Fig. 3C, the back of the silicon substrate 101 is subjected to CMP in the same manner, whereby the back of the substrate is polished to the slice grooves 104. Thereby, the substrate is separated into individual solid-state imaging devices. As mentioned above, after having been mounted in a collective manner, the elements are separated from each other without involvement of positioning of individual elements and electrical connection, such as wire bonding. Therefore, manufacture of the elements is easy, and the elements are easy to handle.

[0072] The trench sections 204 are formed in advance in the glass substrate 201. After mounting of the elements, the substrate is removed from the surface to the depth arriving at the trench sections 204 by means of a method, such as CMP. Hence, separation of the elements can be performed very easily. Further, The edge of the glass substrate 201 is placed inside with reference to the edge of the silicon substrate 101 having the solid-state imaging elements formed therein, and the surface of the silicon substrate 101 becomes exposed. Such a structure can be formed with high accuracy through very simple processes; that is, a process of forming indentations in the glass substrate beforehand and a process of removing the substrate to this depth by means of a method, such as etchback or CMP after bonding operation. Further, the structure can be formed readily with superior operability. Individual solid-state imaging elements can be formed by means of performing only separating or abrading operation while an element-formed surface is sealed within the gap C by means of bonding. Hence, highly-reliable solid-state imaging elements can be provided without inflicting much damage to the elements and without a chance of mixing of dust.

[0073] Moreover, the silicon substrate is reduced in thickness to a depth about half its original depth by means of CMP, and hence an attempt can be made to make the solid-state imaging element compact and thin. Moreover, after having been bonded to the glass substrate, the silicon substrate is made thin, and hence a drop in mechanical strength of the substrate can be prevented.

[0074] Further, connection with the outside can be readily effected, because the bonding pads BP provided on the silicon substrate constituting the solid-state imaging element substrate 100 are exposed by way of the sealed section formed by the spacer 203S and the glass substrate 201.

[0075] As mentioned above, according to the configuration of the present invention, positioning is performed on the wafer scale, and elements are mounted in a collective manner, whereby the substrate and the cover glass are integrated together. Then, the substrate is separated on a per-solid-state-imaging-element basis. Hence, a highly-reliable solid-state imaging device which is easy to manufacture can be formed.

[0076] In the first embodiment, a wiring layer including a bonding pad is formed from a gold layer. However, the material of the wiring layer is not limited to gold. Needless to say, another metal such as aluminum or another conductor layer such as silicide may be used.

The microlens array can also be formed by means of forming a transparent resin film on the surface of a substrate and forming a lens layer having a gradient of refractive index at a predetermined depth, caused by migration of ions from the surface of the resin film.

[0077] The material for the spacer can be selected from any of a 42 alloy, metal, glass, photosensitive polyimide,

and polycarbonate resin, as well as a silicon substrate, as required. When resin is employed, a device is required to ensure a sufficient thickness.

[0078] When the solid-state imaging element substrate, the spacers, and the glass substrate differ from each other in terms of coefficient of linear expansion, warpage may arise in the substrate after adhesion. In order to prevent occurrence of a warpage and bring a warpage into an allowable range even when the warpage has arisen, a bonding (connecting) temperature employed for bonding is set to room temperature or so; specifically, within a range of 20°C to 80°C. The adhesive employed in the present embodiment includes epoxy-based adhesives, oxelane-based adhesives, silicon-based adhesives, and acrylic adhesives; UV curing type adhesives; and visible ray curing type adhesives. An adhesive which can be used in the form of a thin adhesive layer is desirable so that achievement of desired bonding strength, prevention of intrusion of moisture, and attainment of high reliability can be implemented.

[0079] In the first embodiment, the manner in which warpage arises as a result of a bonding temperature having been changed is determined. Tests were carried out by means of observing how warpage arises when bonding is performed through use of the room temperature curing type adhesive and the thermosetting type adhesive with respect to respective cases where the bonding temperature was varied among 20°C, 25°C, 50°C, 80°C, and 100°C. The tests were carried out in connection with bonding between the glass substrate and the spacers and with bonding between the spacers and the solid-state imaging element substrate.

[0080] The test results show that the manner of occurrence of warpage when bonding is performed through use of the room temperature curing type adhesive is analogous to that when bonding is performed through use of the adhesive of thermosetting type. Warpage hardly occurred when the bonding temperature was 20°C and 25°C. When the bonding temperature was 50°C, warpage sometimes occurred, but the warpage fell within the allowable range. When the bonding temperature exceeded 80°C, warpage falling within the allowable range often occurred. When the bonding temperature was 100°C, the warpage became large and sometimes exceeded the allowable range.

[0081] The test results indicate that the bonding temperature preferably should not exceed 80°C.

[0082] When the photocuring type adhesive is used, the bonding temperature does not exceed 50°C. Hence, a superior bonding state can be attained without occurrence of warpage.

[0083] Moreover, simulation was conducted with a view toward determining optimum distance between the sensor and the glass. Conditions for simulation include an exit pupil of 3.5 mm, an F value of 3.5, and a glass refractive index of 1.5.

[0084] When an imperfection measuring 5 μm existed in the lower surface of the glass substrate, a distance between the light-receiving surface of the photodiode section of the solid-state imaging element and the lower surface of the substrate was changed, whereby a relationship between the distance and the density of a shadow of the imperfection projected on the solid-state imaging element was measured. Simulation results are provided in Table 1.

[0085] As is evident from Table 1, when the distance between the light-receiving surface and the glass substrate is 0.07 mm, the density of the shadow becomes 4.7%, which is in excess of 4%. Accordingly, the distance between the light-receiving surface and the glass substrate is desirably set to 0.08 mm or more.

TABLE 1

DISTANCE BETWEEN LOWER SURFACE OF GLASS SUBSTRATE AND LIGHT-RECEIVING SURFACE (mm)	DENSITY OF SHADOW OF IMPERFECTION IN LOWER SURFACE PROJECTED ON CCD (%)
0.01	
0.02	
0.03	
0.04	
0.05	8.3
0.06	6.1
0.07	4.7
0.08	3.7
0.09	3.0
0.1	2.5

[0086] Table 2 shows results of measurement of a relationship between the distance and the density of a shadow projected on the solid-state imaging element for the case where the distance between the light-receiving surface and an upper surface of the glass substrate was changed and an imperfection measuring 20 μm existed in the upper surface of the glass substrate.

TABLE 2

DISTANCE BETWEEN LIGHT-RECEIVING SURFACE AND UPPER SURFACE OF GLASS SUBSTRATE (mm)	DENSITY OF SHADOW OF IMPERFECTION IN UPPER SURFACE PROJECTED ON CCD (%)
0.3	8.3
0.4	5.1
0.5	3.5
0.6	2.5
0.7	1.9
0.8	1.5
0.9	1.2
1.0	1.0
1.1	0.8

[0087] As is evident from the table, the density of the shadow becomes 4% or more when the distance between the light-receiving surface and the upper surface of the glass substrate is 0.4 mm or less.

[0088] When the background is uniform, such as when the sky serves as the background, the density of the shadow projected on the light-receiving surface of the solid-state imaging element is 4%. The background becomes visible in a printed image. Therefore, when the density of the shadow is set to a value of 4% or less, the printed image is not affected by the influence of such an imperfection.

[0089] The test results show that the interval between the surface of the glass substrate and the CCD must be 0.08 mm or more. Preferably, the glass substrate and the CCD are separated from each other by 0.12 mm or thereabouts.

[0090] Even when a piece of debris measuring 20 μ m is on the surface of the glass substrate, the required distance or thickness from the light-receiving surface to the upper surface of the glass substrate is only 0.5 mm or more.

[0091] Moreover, similar simulation yields the result that the required distance from the light-receiving surface to the upper surface of the glass substrate should be only 1.5 mm or more at an F value of 11. From the above-described results, if the distance from the light-receiving surface to the upper surface of the glass substrate is set to 0.5 mm to 1.5 mm, occurrence of image noise can be prevented even when there are pieces of debris which are too small to be visually perceived. Further, the distance from the light-receiving surface to the surface of the glass substrate is desirably 1.5 mm or less, in consideration of a problem related to the size of the device and deterioration of dicing productivity due to a large thickness of glass.

(Second Embodiment)

[0092] A second embodiment of the present invention will now be described.

[0093] In the first embodiment, the slice grooves 104 have been formed, in advance, in the silicon substrate 101 constituting the solid-state imaging element substrate 100. Through use of a spacer which is formed from the same silicon as that of the solid-state imaging element substrate and has a thickness of 0.1 mm, the solid-state imaging element substrate is bonded to the sealing cover glass made of low α -ray glass. The back of the silicon substrate 101 is subjected to CMP until the slice grooves 104 are reached, thereby separating the silicon substrate 101 while rendering the same thin. The present embodiment is characterized in that the silicon substrate 101 is separated without formation of slice grooves. In other respects, the second embodiment is formed in the same manner as in the first embodiment.

[0094] Figs. 4A to 4D show bonding and separation processes of the second embodiment. As shown in Fig. 4A, the silicon substrate 101 is taken as a starting material. A channel stopper, a channel region, and the element region 102, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0095] Subsequently, as shown in Fig. 4B, positioning is performed by means of alignment marks formed in the outer edge of each substrate, and the sealing cover glass 200 is placed on the solid-state imaging element substrate 100 having the element regions formed therein, in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. At this time, no slice grooves are formed in the silicon substrate 101, and hence high mechanical strength is achieved.

[0096] As shown in Fig. 4C, the back of the glass substrate 201 is subjected to CMP (chemical-mechanical polishing) in the same manner as in the case of the first embodiment, whereby the back of the glass substrate 201 is removed to the trench section 204. Thereby, the substrate is separated into individual solid-state imaging devices.

[0097] Through these processes, a reduction in the thickness of the glass substrate 201 and separation of the glass substrate into pieces can be achieved simultaneously.

[0098] As shown in Fig. 4D, the silicon substrate 101 is sliced apart by means of a diamond blade (grindstone), whereby solid-state imaging devices are separated from each other.

[0099] According to this method, the solid-state imaging device produced in the present embodiment is larger in thickness than the solid-state imaging device produced in the first embodiment. However, highly reliable solid-state imaging devices can be formed.

(Third Embodiment)

[0100] A third embodiment of the present invention will now be described.

[0101] In the first embodiment, the slice grooves 104 have been formed, in advance, in the silicon substrate 101 constituting the solid-state imaging element substrate 100. After bonding operation, the back of the silicon substrate 101 is subjected to CMP until the slice grooves 104 are reached, thereby separating the silicon substrate 101 while rendering the same thin. However, in the present embodiment, a dummy plate 301 made of a silicon substrate having a thickness of 50 to 700 μm is caused to adhere to the back of the silicon substrate 101 by way of an adhesive layer 302. After adhesion of the dummy plate, slice grooves 304 are formed in the dummy plate 301 to a depth reaching the dummy plate 301.

[0102] Accordingly, the adhesive layer 302 may be softened in theseparationprocesstodeprivetheadhesive-layeroftackiness, thereby removing the dummy plate 301.

[0103] In other respects, the third embodiment is formed in the same manner as in the first embodiment.

[0104] Figs. 5A to 5E show bonding and separation processes of the third embodiment. The silicon substrate 101 is taken as a starting material. A channel stopper, a channel region, and the element region, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer. Subsequently, as shown in Fig. 5A, the dummy plate 301 made of a silicon substrate is caused to adhere to the back of the silicon substrate 101 by way of the adhesive layer 302.

[0105] As shown in Fig. 5B, the slice grooves 304 are formed from the element-formed surface side of the silicon substrate 101 through use of a diamond blade (grindstone).

[0106] Subsequently, as shown in Fig. 5C, positioning is performed by means of alignment marks (not shown) formed in the outer edge of the solid-state imaging element substrate 100 and that of the sealing cover glass 200, and the sealing cover glass 200 made of low α -ray glass is placed on the solid-state imaging element substrate 100 that has been formed in the manner as mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. Here, a glass substrate having the spacer 203S, which has been formed through the processes shown in Figs. 2A to 2C and has a thickness of 0.1 mm, and the adhesive layer 207 of room temperature curing type is used as the glass substrate. Although the slice grooves 304 are formed so as to penetrate through the silicon substrate 101 at this time, the silicon substrate is fixed by the dummy plate 301, and hence high mechanical strength is achieved.

[0107] As shown in Fig. 5D, the back of the glass substrate is subjected to CMP (chemical-mechanical polishing) in the same manner as in the case of the first embodiment, whereby the back of the glass substrate 201 is removed to the trench section 204.

[0108] Through these processes, a reduction in the thickness of the glass substrate and separation of the glass substrate into pieces can be achieved simultaneously.

[0109] As shown in Fig. 5E, the adhesive layer 302 provided on the back of the silicon substrate 101 is softened to remove the dummy plate 301, whereby the solid-state imaging devices are separated from each other. Here, a material whose softening point is lower than that of the adhesive layer 202 to be used for bonding the spacer to the glass substrate 201 is preferably selected as the adhesive layer 302.

[0110] According to this method, the solid-state imaging element substrate 100 is subjected to dicing in advance on the dummy plate 301 before being bonded. Hence, the solid-state imaging device of the present embodiment undergoes less stress after bonding than does the solid-state imaging device obtained in the first embodiment, and hence a manufacturing yield is improved. Moreover, an attempt can be made to improve the reliability of the solid-state imaging element.

[0111] In the embodiment, the glass substrate and the spacer may be bonded together through use of the adhesive layer. However, the bonding can also be realized by means of anodic bonding or surface activation room temperature bonding. Anodic bonding enables easy achievement of sturdy bonding.

[0112] CMP has been used for reducing the thickness of the glass substrate in the first through third embodiments. However, a grinding method, a polishing method, and an etching method are also applicable.

(Fourth Embodiment)

[0113] A fourth embodiment of the present invention will now be described.

[0114] In the first embodiment, the trench sections 204 have been formed, in advance, in areas corresponding to inter-element regions of the glass substrate 201, constituting the sealing cover glass 200 made of low α -ray glass. After the solid-state imaging element substrate has been bonded to the glass substrate, the back of the glass substrate 201 is subjected to CMP, thereby separating the elements from each other. The present embodiment is characterized in that a glass substrate having no indentation sections formed therein is bonded to the solid-state imaging element substrate; and in that, at the time of separation of the elements, the neighborhood of the separation lines is evaporated by means of dicing or a laser, thereby adjusting the edges of the glass substrates 201 of the respective solid-state imaging elements so as to come to an inner position with reference to the edge of the silicon substrate 101 constituting the solid-state imaging element substrate 100. In other respects, the fourth embodiment is formed in the same manner as in the first embodiment.

[0115] According to this method, as shown in Fig. 2B, processing of the glass substrate is terminated at a point in time when the spacer having a thickness of 0.1 mm is formed. A glass substrate formed by bonding the spacer 203S to the flat glass substrate 201 is used as starting material.

[0116] As shown in Fig. 6A, the silicon substrate 101 (a 6-inch wafer is employed herein) is prepared beforehand, and the slice grooves 104 are formed in areas corresponding to separation lines, which are to be used for separating solid-state imaging elements, on the surface of the silicon substrate 101, by means of a method such as etching. Formation of a channel stopper layer, formation of channel regions, and formation of element regions, such as charge transfer electrodes, are performed through use of ordinary silicon processes. A wiring layer is also formed in the surface, and the bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0117] Subsequently, as shown in Fig. 6B, positioning is performed by means of alignment marks formed in the outer edge of each substrate, and the sealing cover glass 200 is placed on the solid-state imaging element substrate 100 formed in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type.

[0118] Subsequently, as shown in Fig. 6C, the neighborhood of the separation lines is evaporated from the back of the glass substrate by means of dicing or laser, and separation is performed by means of adjusting the edges of the glass substrates 201 of the respective solid-state imaging elements so as to come to an inner position with reference to the edge of the silicon substrate 101 constituting the solid-state imaging element substrate 100.

[0119] As shown in Fig. 6D, the back of the silicon substrate 101 is subjected to CMP in the same manner, and the back of the silicon substrate is polished to the slice grooves 104, thereby separating the solid-state imaging devices from each other. This process is not limited to CMP, but grinding polishing, or etching may also be employed.

[0120] As mentioned above, the solid-state imaging devices are separated from each other after having been mounted in a collective manner. Hence, the solid-state imaging devices are easy to manufacture and handle.

[0121] The trench sections 204 are not formed beforehand in the glass substrate 201, and the edges of the glass substrate 201 are removed by means of evaporation through use of dicing or a laser. Hence, separation can be realized very easily.

[0122] As mentioned above, a structure, wherein the edge of the glass substrate 201 is placed inside with reference to the edge of the silicon substrate 101 having the CCDs mounted thereon, to thus expose the surface of the silicon substrate 101, can be formed with high accuracy through a simple process, such as evaporation due to dicing or a laser.

[0123] Since the glass substrate maintains the same thickness until a separation process, warpage or distortion can be reduced.

(Fifth Embodiment)

[0124] A fifth embodiment of the present invention will now be described.

[0125] In the fourth embodiment, the slice grooves 104 have been formed, in advance, in the silicon substrate 101 constituting the solid-state imaging element substrate 100. After bonding operation, the back of the silicon substrate 101 is subjected to CMP until the slice grooves 104 are reached, thereby separating the silicon substrate 101 while rendering the same thin. However, the present embodiment is characterized in that the silicon substrate 101 is separated without forming slice grooves and the thickness of the silicon substrate is left exactly as is. As in the case of the fourth embodiment, the glass substrate 201 is bonded to the silicon substrate 101 without forming the trench sections 204 in the glass substrate 201, and the edges are evaporated at the time of separation operation. In other respects, the fifth embodiment is formed in the same manner as in the first embodiment.

[0126] Figs. 7A to 7D show bonding and separation processes of the second embodiment. As shown in Fig. 7A, the silicon substrate 101 is taken as a starting material. A channel stopper, a channel region, and the element region 102, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is

also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0127] Subsequently, as shown in Fig. 7B, positioning is performed by means of alignment marks formed in the outer edge of each substrate, and the sealing cover glass 200 is placed on the solid-state imaging element substrate 100 having the element regions formed therein, in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. At this time, no slice grooves and no indentation sections are formed in the silicon substrate 101 and the glass substrate 201, and hence high mechanical strength is achieved.

[0128] Subsequently, as shown in Fig. 7C, the neighborhood of the separation lines is evaporated from the back of the glass substrate by means of dicing or a laser, as in the case of the fourth embodiment. Separation is performed by means of adjusting the edges of the glass substrates 201 of the respective solid-state imaging elements so as to come to an inner position with reference to the edge of the silicon substrate 101 constituting the solid-state imaging element substrate 100.

[0129] Finally, as shown in Fig. 7D, the solid-state imaging element substrate is cut from the part of the glass substrate 201 through use of a diamond blade (grindstone), thereby separating the solid-state imaging devices from each other.

[0130] According to this method, the solid-state imaging device produced in the present embodiment is larger in thickness than the solid-state imaging device produced in the first embodiment. However, highly reliable solid-state imaging devices can be formed.

(Sixth Embodiment)

[0131] A sixth embodiment of the present invention will now be described.

[0132] In the fourth embodiment, the slice grooves 104 have been formed, in advance, in the silicon substrate 101 constituting the solid-state imaging element substrate 100, and the back of the silicon substrate 101 is subjected to CMP, thereby separating the silicon substrate 101. Moreover, in the fifth embodiment, the separation slices 104 are not formed beforehand in the silicon substrate 101 constituting the solid-state imaging element substrate 100. After bonding operation, the silicon substrate 101 is separated through use of the diamond blade (grindstone), thereby separating the silicon substrate 101. However, in the present embodiment, the dummy plate 301 made of a silicon substrate having a thickness of 50 to 700 μm is caused to adhere to the back of the silicon substrate 101 by way of the adhesive layer 302, to thereby obviate a necessity for separating the silicon substrate 101 after the sealing cover glass 200 has been bonded to the solid-state imaging element substrate 101. After adhesion of the dummy plate, the slice grooves 304 are formed in the dummy plate 301 to the depth reaching the dummy plate 301.

[0133] Accordingly, the adhesive layer 302 may be softened in the separation process to deprive the adhesive layer of tackiness, thereby removing the dummy plate 301.

[0134] In other respects, the sixth embodiment is formed in the same manner as in the fourth and fifth embodiments.

[0135] Figs. 8A to 8E show bonding and separation processes of the sixth embodiment. The silicon substrate 101 is taken as a starting material. A channel stopper, a channel region, and the element region, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer. Subsequently, as shown in Fig. 8A, the dummy plate 301 made of a silicon substrate having a thickness of 50 to 700 μm is caused to adhere to the back of the silicon substrate 101 by way of the adhesive layer 302.

[0136] As shown in Fig. 8B, the slice grooves 304 are formed from the element-formed surface side of the silicon substrate 101 through use of a diamond blade (grindstone).

[0137] Subsequently, as shown in Fig. 8C, positioning is performed by means of alignment marks (not shown) formed in the outer edge of the solid-state imaging element substrate 100 and that of the sealing cover glass 200, and the sealing cover glass 200 made of low α -ray glass is placed on the solid-state imaging element substrate 100 that has been formed in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. Here, a glass substrate, in which the spacer 203S having a thickness of 0.1 mm is formed by means of patterning the silicon substrate formed on the glass substrate 201 in the same manner as in the processes shown in Figs. 2A to 2C, is used as the glass substrate 201 serving as the sealing cover glass 200. The adhesive layer 207 of room temperature curing type is formed on the end face of the spacer 203S. Although the slice grooves 304 are formed so as to penetrate through the silicon substrate 101 at this time, the silicon substrate is fixed by the dummy plate 301, and hence high mechanical strength is achieved.

[0138] As shown in Fig. 8D, the neighborhood of the separation lines is evaporated from the back of the glass substrate by means of dicing or a laser in the same manner as in the case of the fourth embodiment, and separation is performed by means of adjusting the edges of the glass substrates 201 of the respective solid-state imaging elements so as to come to an inner position with reference to the edge of the silicon substrate 101 constituting the solid-state

imaging element substrate 100.

[0139] As shown in Fig. 8E, the adhesive layer 302 provided on the back of the silicon substrate 101 is softened to remove the dummy plate 301, whereby the solid-state imaging devices are separated from each other. Here, a material whose softening point is lower than that of the adhesive layer 202 to be used for bonding the spacer to the glass substrate 201 is preferably selected as the adhesive layer 302.

[0140] According to this method, the solid-state imaging element substrate 100 is subjected to dicing in advance on the dummy plate 301 before being bonded. Hence, the solid-state imaging device of the present embodiment undergoes less stress after bonding than does the solid-state imaging device obtained in the first embodiment, and hence a manufacturing yield is improved. Moreover, an attempt can be made to improve the reliability of the solid-state imaging element.

[0141] In the fourth through sixth embodiments, cutting of the glass substrate may be performed by means of scribing or etching.

(Seventh Embodiment)

[0142] A seventh embodiment of the invention will now be described. In the sixth embodiment, the dummy plate 301 made of a silicon substrate having a thickness of 50 to 700 μm is caused to adhere to the back of the silicon substrate 101 by way of the adhesive layer 302. After adhesion of the dummy plate, the slice grooves 304 are formed in the dummy plate 301 to the depth reaching the dummy plate 301. After the silicon substrate 101 has been bonded to the glass substrate 201, the adhesive layer 302 is softened in the process of separating the solid-state imaging element substrate into individual solid-state imaging elements, and the solid-state imaging elements are separated by means of removing the dummy plate 301. In the present embodiment, a dummy plate 401 made of a silicon substrate having a thickness of 50 to 700 μm is caused to adhere to the back of the glass substrate 201 by way of an adhesive layer 402. After adhesion of the dummy plate, indentation sections 404 are formed to a depth reaching the dummy plate 401. After the silicon substrate 101 has been bonded to the glass substrate 201, the adhesive layer 402 is softened in the process of separating the solid-state imaging element substrate into individual solid-state imaging elements, and the solid-state imaging elements are separated by means of removing the dummy plate 401. In other respects, the solid-state imaging elements are formed in the same manner as in the sixth embodiment.

[0143] As in the case of the second and fourth embodiments, a silicon substrate for which neither separation grooves nor a dummy plate are formed is used as the silicon substrate 101 constituting the solid-state imaging element substrate 100. Finally, the silicon substrate is sliced and separated by means of the diamond blade (grindstone).

[0144] The bonding and separation processes are shown in Figs. 9A through 9E.

[0145] As shown in Fig. 9A, the dummy plate 401 made of a silicon substrate having a thickness of 50 to 700 μm is caused to adhere to the back of the glass substrate 201 by way of the adhesive layer 402. After adhesion of the dummy plate, the silicon substrate 203 is caused to adhere to the adhesive layer 402 by way of the adhesive layer 202. As in the case of the first embodiment described by reference to Figs. 2A through 2C, the silicon substrate 203 is subjected to etching using photolithography, to thus form the spacer 203S having a thickness of 0.1 mm.

[0146] As shown in Fig. 9B, as in the case of the first embodiment, the areas corresponding to the regions between the solid-state imaging elements are again selectively etched, thereby forming the indentation sections 404 having a depth reaching the dummy plate 401. Moreover, the indentation sections may be formed by means of half-dicing.

[0147] The silicon substrate 101 is taken as a starting material. A channel stopper, a channel region, and the element region, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer. Subsequently, as shown in Fig. 9C, positioning is performed by means of alignment marks (not shown) formed in the outer edge of the solid-state imaging element substrate 100 and that of the sealing cover glass 200 made of low α -ray glass. The sealing cover glass 200 having the dummy plate 401 is placed on the solid-state imaging element substrate 100 that has been formed in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type.

[0148] As shown in Fig. 9D, the adhesive layer 402 is softened by means of heating, thereby removing the dummy plate 401. As a result, the glass substrate 201 is separated.

[0149] As shown in Fig. 9E, the solid-state imaging element substrate made of the silicon substrate 101 is sliced through use of the diamond blade (grindstone), thereby separating the solid-state imaging devices from each other.

[0150] According to this method, the glass substrate 201 constituting the sealing cover glass 200 is sliced in advance on the dummy plate 401 by means of dicing or etching before being bonded. Hence, the solid-state imaging device of the present embodiment undergoes less stress after bonding than does the solid-state imaging device obtained in the first embodiment, and hence a manufacturing yield is improved. Moreover, an attempt can be made to improve the reliability of the solid-state imaging element.

(Eighth Embodiment)

[0151] An eighth embodiment of the present invention will now be described.

[0152] In the seventh embodiment, the silicon substrate 101 constituting the solid-state imaging element substrate 100 is subjected to bonding in its present form without forming the slice grooves 104 in the silicon substrate beforehand. Finally, the solid-state imaging element substrate is sliced by means of the diamond blade (grindstone). However, the present embodiment is characterized in that the slice grooves 104 have been formed in advance in the silicon substrate 101 constituting the solid-state imaging element substrate 100 and in that the silicon substrate is polished from the back thereof, by means of CMP after bonding until the substrate is polished to the slice grooves 104, thereby separating the silicon substrate 101 while reducing the thickness of the same. In other respects, the eighth embodiment is formed in the same manner as in the seventh embodiment.

[0153] Specifically, Figs. 10A to 10D show bonding and separation processes of the eighth embodiment. As shown in Fig. 10A, the silicon substrate 101 having the slice grooves 104 formed therein is taken as a starting material. A channel stopper, a channel region, and the element region 102, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0154] Subsequently, as shown in Fig. 10B, positioning is performed by means of alignment marks formed in the outer edges of the respective substrates, and the sealing cover glass 200 (with the dummy substrate 401) made of low α -ray glass in the manner as described in the seventh embodiment is placed on the solid-state imaging element substrate 100. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type.

[0155] As shown in Fig. 10C, the back of the solid-state imaging element substrate 100 is subjected to CMP (chemical-mechanical polishing), whereby the back of the silicon substrate 101 is removed to the slice grooves 104.

[0156] Through these processes, a reduction in the thickness of the solid-state imaging element substrate and separation of the glass substrate into pieces can be achieved simultaneously. Even in this case, grinding, polishing, or etching may be employed in place of CMP.

[0157] As shown in Fig. 10D, the adhesive layer 402 may be heated and softened, thereby removing the dummy plate 401.

(Ninth Embodiment)

[0158] A ninth embodiment of the present invention will now be described.

[0159] In the seventh embodiment, the silicon substrate 101 constituting the solid-state imaging element substrate 100 is subjected to bonding in its present form without the slice grooves 104 being formed in the silicon substrate beforehand. Finally, the solid-state imaging element substrate is sliced by means of the diamond blade (grindstone). However, in the present embodiment, a dummy plate has been formed in advance in the silicon substrate 101 constituting the solid-state imaging element substrate 100 and in the glass substrate 201 constituting the sealing cover glass 200. Before bonding operation, the slice grooves 104 and the trench sections 204 have been formed. After bonding operation, the adhesive layers 402 and 302 are separated from each other by means of removing the dummy plates 301 and 401. In other respects, the ninth embodiment is formed in the same manner as in the seventh embodiment.

[0160] Specifically, Figs. 11A to 11D show bonding and separation processes of the ninth embodiment. The silicon substrate 101 having the dummy plate 301 bonded thereon is taken as a starting material. A channel stopper, a channel region, and the element region 102, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0161] As shown in Fig. 11B, the slice grooves 304 are formed in the dummy plate 301 to reach the dummy plate 301.

[0162] As in the case of the seventh and eighth embodiments, the dummy plate 401 is caused to adhere to the sealing cover glass 200, and the indentation sections 404 are formed by means of etching or dicing.

[0163] Subsequently, as shown in Fig. 11C, positioning is performed by means of alignment marks formed in the outer edges of the respective substrates, and the sealing cover glass 200 that has the dummy substrate 401 and is formed as in the seventh embodiment is placed on the solid-state imaging element substrate 100 with the dummy substrate 301. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type.

[0164] As shown in Fig. 11D, the adhesive layers 402 and 203 are softened to remove the dummy plates 301, 401, thereby separating the solid-state imaging elements into pieces.

[0165] Adhesives having substantially the same softening temperature are used for the adhesive layers 302, 402 and may be softened simultaneously.

[0166] After one of the two adhesive layers has been softened and removed, the substrate from which the adhesive

layer has been removed may be fixed by means of taping, and the remaining adhesive layer may be removed by means of softening.

[0167] By means of this configuration, the solid-state imaging elements are not susceptible to excessive stress after bonding, thereby reducing damage inflicted on the solid-state imaging elements.

(Tenth Embodiment)

[0168] A tenth embodiment of the invention will now be described.

[0169] As shown in Figs. 2A and 2B, in the first through ninth embodiments, at the time of formation of the sealing cover glass 200 in which the spacer 203S having a thickness of 0.1 mm is formed, the silicon substrate 203 which is to become a spacer is caused to adhere to the glass substrate 201 by way of an adhesive. The silicon substrate 203 is patterned by means of the etching method using photolithography, and the slice grooves 104 are formed. However, in the present embodiment, as shown in Figs. 12A and 12B, the spacers 203S are etched on a dummy plate 501. Subsequently, the spacers 203S are caused to adhere to the glass substrate 201 by way of the adhesive layer 202.

[0170] As shown in Fig. 12A, the silicon substrate 203, which is to become spacers, is caused to adhere to the dummy plate 501 made of a silicon substrate by way of an adhesive layer 502 having a softening temperature of 50°C to 150°C or thereabouts. The silicon substrate 203 is patterned by means of the etching method using photolithography, thereby forming the spacers 203S.

[0171] As shown in Fig. 12B, the glass substrate 201 is caused to adhere to the spacer 203S by way of the adhesive layer 202 having a softening temperature of 100 to 200°C or thereabouts.

[0172] After adhesion of the glass substrate 201, the substrates are heated to a temperature at which the adhesive layers 202 are not softened but the adhesive layer 502 becomes soft (i.e., about 50 to 150°C or thereabouts), thereby softening the adhesive layer 502 to remove the dummy plate 501. Thereby, the sealing cover glass 200 with the spacer is formed.

[0173] This method does not need to process the spacers on the glass substrate, thereby preventing occurrence of flaws in the glass substrate 201, which would otherwise be responsible for fogging.

[0174] The adhesive layer 502 to be used for the dummy plate should withstand a baking temperature employed in the photolithography. Because of a necessity for removing the dummy plate 501, the adhesive layer 202 to be used for causing the spacer 203S to adhere to the glass substrate 201 must be sufficiently higher in softening temperature than the adhesive layer 502.

[0175] When indentation sections must be formed in the glass plate, the trench sections 204 should have been formed by means of dicing or etching before adhesion of the adhesive layer, as shown in Fig. 13. After removal of the dummy plate 501, projections and indentations should be formed by means of dicing or etching.

[0176] The slicing and cutting processes are the same as those shown in Figs. 3 through 5, which have been described in connection with the first through third embodiments.

(Eleventh Embodiment)

[0177] An eleventh embodiment of the present invention will now be described.

[0178] In the first through tenth embodiments, the spacer 203S are formed separately and are caused to adhere by way of the adhesive layer. However, in the present embodiment, spacers 206 are formed by means of forming indentation sections 205 in the glass substrate 201 made of low α -ray glass, by means of the etching method using photolithography. In other respects, the eleventh embodiment is formed in the same manner as in the previous embodiments.

[0179] Specifically, as shown in Fig. 14A, the glass substrate 201 is prepared.

[0180] As shown in Fig. 14B, the indentation sections 205 are formed by means of the etching method using photolithography, thereby forming a glass substrate provided with spacers 206.

[0181] By means of the configuration, the spacers 206 are formed integrally, and hence manufacture is easy, and no positional displacement arises. Further, there is no chance of distortion arising in the bonded section.

(Twelfth Embodiment)

[0182] A twelfth embodiment of the invention will now be described.

[0183] The eleventh embodiment has described a method for forming the sealing cover glass 200 with which the spacers 206 having a thickness of 0.1 mm are formed integrally. However, as shown in Figs. 15A to 15C, the trench sections 204 can also be formed beforehand by means of etching.

[0184] In the present embodiment, the indentation sections 205 are formed in the glass substrate 201 by means of the etching method using photolithography, thereby forming the spacers 206 integrally. The trench sections 204 of the

glass substrate are also formed by means of etching. Accordingly, occurrence of distortion is diminished, thereby facilitating the separation process.

[0185] Specifically, as shown in Fig. 15A, the glass substrate 201 is prepared.

[0186] As shown in Fig. 15B, the indentation sections 205 are formed in the glass substrate 201 by means of the etching method using photolithography.

[0187] Subsequently, as shown in Fig. 15C, the glass substrate 201 is etched further deeper by means of the etching method using photolithography, to thus form the trench sections 204 and form the spacers 206 integrally.

[0188] These processing steps differ from each other in terms of an etch depth and, hence, require two etching operations. The resist pattern which is to become a mask may be formed into a double-layer structure. According to one possible method, after etching of the trench sections 204 to be used for forming spacers, only the upper resist pattern is selectively removed, to thus perform etching while only the lower resist pattern is taken as a mask.

[0189] The bonding and separation processes are the same as the those shown in Figs. 3 through 5 which have been described in connection with the first through third embodiments.

(Thirteenth Embodiment)

[0190] A thirteenth embodiment of the present invention will now be described.

[0191] The eleventh and twelfth embodiments have described the method for forming the sealing cover glass 200 with which the spacer 206 having a thickness of 0.1 mm is formed integrally. However, as shown in Figs. 16A to 16D, the silicon substrate 203 for a spacer is caused to adhere to the glass substrate 201 in which the trench sections 204 are formed. The substrates may then be selectively removed by means of the etching method using photolithography, to thus form the spacers 203S. In other respects, the thirteenth embodiment is formed in the same manner as are the eleventh and twelfth embodiments.

[0192] In the present embodiment, the trench sections 204 are formed in the glass substrate 201 by means of the etching method using photolithography. The trench sections 204 of the glass substrate are formed by means of etching. Accordingly, occurrence of distortion is diminished, thereby facilitating the separation process.

[0193] Specifically, as shown in Fig. 16A, the glass substrate 201 is prepared.

[0194] As shown in Fig. 16B, the trench sections 204 are formed in the glass substrate 201 by means of the etching method using photolithography, thereby forming the trench sections 204.

[0195] Subsequently, as shown in Fig. 16C, the silicon substrate 203, which is to serve as a substrate for spacers, is caused to adhere to the glass substrate 201 by way of the adhesive layer 202.

[0196] Further, as shown in Fig. 16D, the spacers 203S are integrally formed by means of the etching method using photolithography.

[0197] By means of the method, the sealing glass cover 200 with highly reliable spacers can be formed with high accuracy.

[0198] The slicing and cutting processes are the same as those shown in Figs. 3 through 5, which have been described in connection with the first through third embodiments.

(Fourteenth Embodiment)

[0199] A fourteenth embodiment of the present invention will now be described.

[0200] As shown in Figs. 16A to 16D, in the thirteenth embodiment, the silicon substrate 203, which has a thickness of 0.1 mm and is to become a spacer, is caused to adhere to the glass substrate 201 by way of the adhesive. The silicon substrate 203 is patterned by means of the etching method using photolithography, thereby forming the sealing cover glass 200 made of low α -ray glass. However, in the present embodiment, as shown in Figs. 17A and 17B, the spacers 203S are etched on the dummy plate 501. Subsequently, the spacers 203S are caused to adhere to the glass substrate 201 having the trench sections 204 formed therein, by way of the adhesive layer 202. In other respects, the tenth embodiment is formed in the same manner as in the thirteenth embodiment.

[0201] Specifically, the silicon substrate 203, which is to become spacers, is caused to adhere to the dummy plate 501 made of a silicon substrate by way of the adhesive layer 502 having a softening temperature from 50°C to 150°C or thereabouts. As shown in Fig. 17A, the silicon substrate 203 is patterned by means of the etching method using photolithography, thereby forming the spacers 203S.

[0202] As shown in Fig. 17B, the glass substrate 201 having the trench sections 204 is caused to adhere to the spacers 203S by way of the adhesive layer 202 having a softening temperature of 100 to 200°C or thereabouts.

[0203] After adhesion of the glass substrate 201, the adhesive layer 502 is heated to 50 to 150°C within a range in which the adhesive layer 202 is not softened, and thereby softened to remove the dummy plate 501, to thus form the sealing cover glass 200 with spacers, as shown in Fig. 17C.

[0204] This method does not require processing the spacers on the glass substrate, thereby preventing occurrence

of flaws in the glass substrate 201, which would otherwise be responsible for fogging.

[0205] The bonding and separation processes are the same as those shown in Figs. 3 through 5, which have been described in connection with the first through third embodiments.

(Fifteenth Embodiment)

[0206] A fifteenth embodiment of the present invention will now be described.

[0207] The twelfth through fourteenth embodiments have described the processes for manufacturing the sealing cover glass 200, which has the trench sections 204 for facilitating the separation process, which has spacers having a thickness of 0.1 mm, and which is made of low α -ray glass. Fifteenth through seventeenth embodiments are characterized in that the glass substrate is separated in advance by means of having caused the dummy plate 401 to adhere to the glass substrate and having formed the trench sections 204; and in that the solid-state imaging elements are separated into pieces by means of softening the adhesive layer 402 after bonding. In other respects, the tenth embodiment is formed in the same manner as in the fourteenth embodiment.

[0208] In the embodiment shown in Figs. 15A through 15C, the trench sections 204 are formed in the glass substrate of the sealing cover glass with integrated spacers, thereby facilitating separation of the glass substrate. However, in the present embodiment, as shown in Fig. 18, separation can be readily effected by means of removing the dummy plate 401 made of the glass substrate, by way of the adhesive layer 402.

[0209] A glass plate is used as starting material. After adhesion of the dummy plate, formation of the trench sections 204 and formation of the spacers 206 are performed by means of the etching method using photolithography.

[0210] By means of this configuration, the only requirement is to soften the adhesive layer 402 at the time of separation, by means of heating. Hence, separation can be attained very easily.

[0211] The bonding and separation processes are the same as those described in connection with the seventh through ninth embodiments.

(Sixteenth Embodiment)

[0212] A sixteenth embodiment of the present invention will now be described.

[0213] The present embodiment is characterized in that the glass substrate 201 is caused to adhere to the dummy plate 401, wherein the glass substrate 201 is of a type which has been described in connection with the thirteenth embodiment and which is formed by causing the spacers 203S having a thickness of 0.1 mm to adhere to the glass plate having indentation sections; in that the trench sections 204 have been formed in the glass substrate 201 beforehand, whereby the glass substrate itself is separated before bonding; and in that, after bonding operation, the adhesive layer 402 is softened, thereby removing the dummy plate to separate the individual solid-state imaging elements.

[0214] In the present embodiment, as shown in Figs. 19A and 19B, the dummy plate 401 is caused to adhere to the glass substrate integrated with the spacers of the embodiment shown in Figs. 16A and 16B by way of the adhesive layer 402, thereby forming the trench sections 204.

[0215] A glass plate is used as starting material. After adhesion of the dummy plate, formation of the trench sections 204 having a depth reaching the dummy plate and formation of the spacers 203S are performed in the same manner as in the thirteenth embodiment.

[0216] As shown in Fig. 19A, the dummy substrate 401 is caused to adhere to the glass substrate 201 by way of the adhesive layer 402.

[0217] As shown in Fig. 19B, the glass substrate 201 is etched through use of photolithography, thereby forming trench sections in the surface of the glass substrate 201 to reach the dummy substrate 401.

[0218] As shown in Fig. 19C, the silicon substrate 203 for spacers is caused to adhere to the glass substrate 201 by way of the adhesive layer 202.

[0219] As shown in Fig. 19D, the silicon substrate 203 is selectively removed by means of the etching method using photolithography, thereby forming the spacers 203S.

[0220] By means of such a configuration, after the glass substrate 201 has been bonded to the solid-state imaging element substrate 100, only the adhesive layer 402 is softened by means of heating at the time of dicing operation, thereby readily separating the solid-state imaging elements.

[0221] The bonding and separation processes are the same as those described in connection with the seventh through ninth embodiments.

(Seventeenth Embodiment)

[0222] A seventeenth embodiment of the present invention will now be described.

[0223] The present embodiment is characterized in that the spacers 203S which have been patterned on the dummy

plate 501 and have a thickness of 0.1 mm and the glass substrate 201 are caused to adhere to the dummy plate 401, wherein the glass substrate 201 is of a type which has been described in connection with the fourteenth embodiment (Fig. 17) and is formed by means of causing the spacers 203S to adhere to the glass plate which is made of low α -ray glass and has the indentation sections where by the glass substrate itself is separated before bonding; and in that, after bonding operation, the adhesive layer 402 is softened, thereby removing the dummy plate to separate the individual solid-state imaging elements. In other respects, the seventeenth embodiment is formed in the same manner as in the fourteenth embodiment.

[0224] In the present embodiment, as shown in Figs. 20A to 20C, the dummy plate 401 is caused to adhere to the glass substrate of spacer adhesion type according to the embodiment shown in Figs. 17A and 17B, by way of the adhesive layer 402.

[0225] A glass plate is used as starting material. After adhesion of the dummy plate, formation of the trench sections 204 having a depth reaching the dummy plate and formation of the spacers 203S are performed in the same manner as in the fifteenth embodiment.

[0226] Specifically, the silicon substrate 203, which is to become spacers, is caused to adhere to the dummy plate 501, which is to become a silicon substrate, by way of the adhesive layer 502. As shown in Fig. 20A, the silicon substrate 203 is patterned by means of the etching method using photolithography, to thus form the spacers 203S.

[0227] As shown in Fig. 20B, the glass substrate 201 having the trench sections 204 formed so as to reach the dummy plate 401 is caused to adhere to the spacers 203S by way of the adhesive layer 402.

[0228] After adhesion of the glass substrate 201 in this manner, the adhesive layer 502 is softened to remove the dummy plate 501. As shown in Fig. 20C, the sealing cover glass 200 with spacers is formed.

[0229] By means of this configuration, the only requirement is to soften the adhesive layer 402 at the time of separation by means of heating. Hence, separation can be attained very easily.

[0230] The bonding and separation processes are the same as those described in connection with the seventh through ninth embodiments.

(Eighteenth Embodiment)

[0231] An eighteenth embodiment of the present invention will now be described.

[0232] The first through seventeenth embodiments have described examples in which the spacers having a thickness of 0.1 mm are formed on a light-transmission substrate. However, eighteenth to twenty-second embodiments will describe examples in which spacers are provided on the solid-state imaging element substrate.

[0233] In the present embodiment, spacers 106S are formed integrally on the silicon substrate 101 constituting the solid-state imaging element substrate. In other respects, the present embodiment is formed in the same manner as the other embodiments.

[0234] As shown in Fig. 21A, a resist pattern is formed on the surface of the silicon substrate 101 by means of photolithography. As shown in Fig. 21B, the indentation sections 105 are formed by means of selective etching while the resist pattern is taken as a mask, thereby forming the spacers 106S.

[0235] As shown in Fig. 21C, a channel stopper layer, a channel region, and the element region 102, such as a charge transfer electrode, are formed in the element formation region enclosed by the spacers 106S through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0236] Subsequently, as shown in Fig. 21D, the glass substrate 201 in which the trench sections 204 is formed from low α -ray glass. As shown in Fig. 21E, the glass substrate 201 is positioned so as to oppose the surface of the solid-state imaging element substrate 100 where elements are formed, to thus integrate the glass substrate 201 and the solid-state imaging element substrate 100 together. At the time of integration, the glass substrate 201 and the solid-state imaging element substrate 100 are firmly integrated together by means of pressurization through use of the adhesive layer 107 of room temperature curing type applied over the surfaces of the spacers.

[0237] Finally, as shown in Fig. 21F, the glass substrate and the solid-state imaging element substrate are made thin by means of CMP, to thus enable separation of solid-state imaging elements. Here, the process for reducing a thickness is not limited to CMP but may be implemented by means of grinding, polishing, or etching.

[0238] When the trench sections 204 are not formed in the glass substrate, the solid-state imaging elements can be separated with superior operability by performing separation through dicing or laser. Moreover, when the slice grooves 104 are not formed in the silicon substrate, the solid-state imaging elements can be separated with superior operability by performing separation through use of a diamond blade.

[0239] According to this method, the spacers are formed integrally with the solid-state imaging element substrate, and hence highly-reliable solid-state imaging devices can be formed without involvement of occurrence of distortion in the bonded section.

(Nineteenth Embodiment)

[0240] A nineteenth embodiment of the present invention will now be described.

[0241] The eighteenth embodiment has described that the spacers having a thickness of 0.1 mm are formed integrally on the solid-state imaging element substrate. However, in the present embodiment, a silicon substrate 103 may be caused to adhere to the solid-state imaging element substrate by way of the adhesive layer 107, and the silicon substrate 108 may be formed as a pattern on the solid-state imaging element substrate. In other respects, the present embodiment is formed in the same manner as the eighteenth embodiment.

[0242] As shown in Figs. 22A through 22C, in the present embodiment, a channel stopper layer, a channel region, and the element region, such as a charge transfer electrode, are formed through use of ordinary silicon processes. Further, a wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0243] As shown in Fig. 22A, the silicon substrate 103 is caused to adhere to the solid-state imaging element substrate by way of an adhesive layer 107.

[0244] Subsequently, as shown in Fig. 22B, the silicon substrate 103 is selectively removed by means of the etching method using photolithography, thereby forming spacers 103S.

[0245] As shown in Fig. 22C, an adhesive layer 109 is applied over the spacers 103S, thereby forming the slice grooves 104.

[0246] According to the method, the spacers are formed after the element regions have been formed on the silicon substrate. Hence, the spacers will not interrupt formation of the element regions, thus facilitating manufacturing operation. Since the spacers are not formed integrally, a problem of occurrence of slight distortion is inevitably raised.

[0247] The bonding and separation processes are the same as those described in connection with the previous embodiments.

(Twentieth Embodiment)

[0248] A twentieth embodiment of the present invention will now be described.

The nineteenth embodiment has described that the spacers 103S having a thickness of 0.1 mm are formed by means of causing the silicon substrate 108 to adhere to the solid-state imaging element substrate by way of the adhesive layer 107 and etching the silicon substrate on the solid-state imaging element substrate. In the present embodiment, the spacers 103 may be formed on a dummy substrate through use of a dummy substrate 601, and the spacers may be caused to adhere to the silicon substrate 101 having the solid-state imaging elements formed therein; that is, a substrate to be used for forming solid-state imaging elements. In other respects, the present embodiment is formed in the same manner as the nineteenth embodiment.

[0249] Specifically, the silicon substrate 103 which is to become spacers is caused to adhere to the dummy plate 601 made of a silicon substrate by way of an adhesive layer 602 having a softening temperature of 50°C to 150°C or thereabouts. The silicon substrate 103 is selectively removed by means of the etching method using photolithography, to thus form the spacers 103S as shown in Fig. 23A.

[0250] As shown in Fig. 23B, the silicon substrate 101 having the solid-state imaging elements formed therein is caused to adhere to the spacers 103S by way of the adhesive layer 202 having a softening temperature of 100 to 200°C or thereabouts.

[0251] After adhesion of the silicon substrate 101 having the solid-state imaging elements formed therein, the adhesive layer 602 is heated to 50 to 150°C or thereabouts and softened, to thus remove the dummy plate 601. As shown in Fig. 23D, the slice grooves 104 are then formed. The solid-state imaging element substrate 100 with spacers is formed in the same manner as shown in Fig. 22B.

[0252] The processes for bonding the glass substrate and the solid-state imaging element substrate together and separating the substrates are the same as those described in connection with the eighteenth embodiment.

[0253] The method obviates a necessity for processing spacers on the solid-state imaging element substrate. Hence, there can be prevented occurrence of a drop in yield, which would otherwise be caused by flaws in the solid-state imaging element substrate.

[0254] In the present embodiment, the slice grooves 104 are formed after formation of the spacers. However, needless to say, the slice grooves 104 may be formed before formation of the spacers.

[0255] In the embodiment, bonding of the glass substrate to the spacers and bonding of the silicon substrate constituting the solid-state imaging elements to the spacers are performed through use of adhesive layers. However, if they are bonded directly together at room temperature through surface activation, sturdy bonding can be attained.

[0256] In the first through twentieth embodiments (excluding the eleventh, twelfth, and fifteenth embodiments), the silicon substrate is used for spacers. However, the spacers are not limited to the silicon substrate, and a 42 alloy whose thermal expansion coefficient is close to that of the solid-state imaging element is also applicable. Alternatively, material

whose thermal expansion coefficient is close to that of the light-transmission substrate may also be employed. Moreover, polyimide resin may also be used. In this case, the spacers become flexible, and there is yielded a distortion absorption effect for countering occurrence of distortion due to temperature changes.

[0257] Further, the spacers may be formed through use of an adhesive tape. In this case, after adhesion of the adhesive tape over the entire substrate, the tape is cut by means of laser machining or the like, whereby high-precision machining becomes possible.

[0258] In the first through twentieth embodiments, the silicon substrate or the glass substrate is used when the dummy plate is employed. However, the invention is not limited to these embodiments, and a metal plate is also usable. Further, a flexible film may also be employed.

[0259] Semi-curing resin, UV curing resin, UV/thermosetting combined-type resin, or thermosetting resin can also be applied to the adhesive layer.

[0260] In addition, a transfer method, screen printing, or a dispense method can be selected as the method for forming the adhesive layer, as required.

[0261] In the eighteenth to twentieth embodiments, the slice grooves are formed before formation of the spacers. However, needless to say, the slice grooves may be formed after formation of the spacers.

(Twenty-First Embodiment)

[0262] A solid-state imaging device equipped with a reinforcing plate will now be described as a twenty-first embodiment of the present invention.

[0263] As shown in Fig. 24, the solid-state imaging device is characterized in that a reinforcing plate 701 made of a silicon substrate is caused to adhere to the back of the silicon substrate 101 constituting the solid-state imaging element substrate 100 of the solid-state imaging device of the first embodiment, by way of a silicon oxide film (not shown). Here, the reinforcing plate 701 whose surface is covered with a silicon oxide film and which is made of a silicon substrate is bonded directly to the solid-state imaging element substrate by means of surface activation room temperature bonding. Even in this case, a distance from the surface of the solid-state imaging element substrate to the surface of the sealing cover glass is 0.6 mm or thereabouts.

[0264] The solid-state imaging device of this embodiment is identical in element configuration with that described in connection with the first embodiment but is characterized in that the back of the silicon substrate is reduced to one-half by means of a CMP method or the like; and in that, in order to compensate for a decrease in the strength of the silicon substrate, the reinforcing plate 701 is bonded to the back of the silicon substrate.

[0265] This configuration enables a reduction in the thickness of the solid-state imaging element substrate 100, an increase in drive speed, and compensation of a decrease in strength attributable to a reduction in thickness, through use of the reinforcing plate. Further, a moisture-proof characteristic is also improved.

[0266] Processes for manufacturing the solid-state imaging device will now be described.

[0267] Processes up to the process for causing the glass substrate made of low α -ray glass to adhere to the solid-state imaging element substrate are basically the same as those described in connection with the first embodiment. Specifically, as shown in Fig. 25A, an element region where solid-state imaging elements are to be formed through use of ordinary silicon processes is formed in the silicon substrate 101 in which the slice grooves 104 have been formed beforehand. A wiring layer is also formed in the surface, and bonding pads BP to be used for establishing an external connection are formed from a gold layer.

[0268] Subsequently, as shown in Fig. 25B, positioning is performed by means of alignment marks formed in the outer edges of the respective substrates, and the sealing cover glass 200 is placed on the solid-state imaging element substrate 100 in which the element region has been formed in the manner as mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. Processing pertaining to this process may be performed through use of a surface activation room temperature bonding.

[0269] As shown in Fig. 25C, the silicon substrate 101 is polished from the back thereof, by means of the CMP method or the like in the same manner until the substrate is polished to the slice grooves 104 while the glass substrate is left exactly as is, thereby separating the solid-state imaging devices from each other.

[0270] As shown in Fig. 25D, the reinforcing plate 701 whose surface is covered with a silicon oxide film (not shown) and which is made of a silicon substrate is bonded directly to the back of the silicon substrate 101 whose thickness has been reduced, by means of surface activation room temperature bonding.

[0271] Finally, the back of the glass substrate 201 is removed to the trench sections 204, thereby reducing the thickness of the glass substrate 201 and separating the solid-state imaging elements apart from each other. Finally, the reinforcing plate is diced through use of a diamond plate (grindstone), thereby forming the solid-state imaging devices, each having the reinforcing plate, as shown in Fig. 25E.

[0272] As mentioned above, the solid-state imaging devices are formed very easily.

[0273] According to the method of the present invention, after the solid-state imaging elements have been mounted in a collective manner, the elements are separated from each other without involvement of electrical connections such as wire bonding. Therefore, manufacture of the solid-state imaging devices is easy, and the solid-state imaging devices are easy to handle. Moreover, the thickness of the silicon substrate is first reduced, to thus separate the solid-state imaging elements. After the reinforcing element has been caused to adhere to the silicon substrate, the reinforcing plate is diced. Therefore, high reliability is achieved.

[0274] Although the spacer formed on the glass substrate is used in the present embodiment, a spacer formed on the solid-state imaging element substrate or a separate spacer may also be applicable. In the present embodiment, the reinforcing plate is formed from a silicon substrate isolated from the solid-state imaging element substrate, thereby imparting heat insulation to the reinforcing plate. However, the reinforcing plate may be utilized as a heatsink through use of a substrate having superior thermal conductivity. In the present embodiment, a damp-proofing characteristic is enhanced. Moreover, the present invention is applicable even when no slice grooves 104 are provided.

(Twenty-Second Embodiment)

[0275] In a twenty-second embodiment of the present invention, as shown in Fig. 26, a metal substrate, such as tungsten or chromium, is caused to adhere in place of the reinforcing plate, thereby realizing a shield plate 801. In other respects, the present embodiment is formed in completely the same manner as are the other embodiments.

[0276] According to this configuration, an electromagnetic wave can be shielded, thereby enabling an attempt to reduce unwanted emission noise.

(Twenty-Third Embodiment)

[0277] A twenty-third embodiment of the present invention will now be described.

[0278] In the first through twenty-second embodiments, the bonding pads are formed on the surface of the solid-state imaging element substrate so as to become exposed. The edge of the light-transmission substrate (i.e., the glass substrate made of low α -ray glass) 201 comes to the inside with reference to the edge of the solid-state imaging element substrate such that electrical connections become possible on the surface of the solid-state imaging element substrate. However, the present embodiment is characterized in that the solid-state imaging element substrate and the glass substrate are formed so as to have identical edges. As shown in Fig. 27C, the present embodiment is also characterized in extraction of signals from the back by way of through holes H formed so as to penetrate through the solid-state imaging element substrate 100 and the reinforcing plate 701 affixed to the back thereof. Reference numeral 108 designates a conductor layer; and 109 designates a silicon oxide layer serving as an insulation layer. The glass substrate 201 serving as a light-transmission member is bonded to the surface of the solid-state imaging element substrate 100 which has the solid-state imaging elements 102 formed thereon and is formed from the silicon substrate 101, the silicon substrate serving as a semiconductor substrate, by way of the spacer 203S having a thickness of 0.1 mm such that the gap C is provided so as to correspond to the light-receiving region of the silicon substrate 101. Signals are extracted from the back of the solid-state imaging element substrate 100 by means of the through holes H formed in the silicon substrate 101. The through hole constitutes a pad 113 and a bump 114, which act as external extraction terminals formed on the back of the solid-state imaging element substrate 100. The outer edge is separated into pieces by means of dicing, and an external connection is established by way of the bump 114. Here, as shown in Fig. 28D, the through hole is connected to a peripheral circuit substrate 901 by way of an anisotropic conductive film 115. In addition to this, diffusion bonding using ultrasonic waves, soldering, and eutectic bonding based on thermocompression bonding are also effective. Moreover, the clearances may be subjected to under-filling with resin. Here, the spacers 203S are set to a height of 30 to 150 μm , preferably a height of 80 to 120 μm . In other respects, the present embodiment is formed in the same manner as is the first embodiment.

[0279] Figs. 27A to 27C and Figs. 28A to 28D show processes for manufacturing the solid-state imaging device.

[0280] Specifically, according to the method, the reinforcing substrate 701, which is provided with a silicon oxide film (not shown) and formed from a silicon substrate, is bonded to the back of the solid-state imaging element substrate 100 by means of surface activation room temperature bonding, wherein the element region to be used for forming solid-state imaging elements and the bonding pads BP to be used for establishing external connections are formed through use of ordinary silicon processes in the same manner as in the processes shown in figs. 6A and 6B (Fig. 27A).

[0281] Subsequently, as shown in Fig. 27B, positioning is performed by means of the alignment marks formed in the outer edges of the respective substrates, and the sealing cover glass 200, in which the spacers 203S are bonded to the flat-plate-like glass substrate 201, is placed on the solid-state imaging element substrate 100 formed in the manner as mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type.

[0282] The through holes are formed from the back of the reinforcing plate 701 by the etching method using photo-

lithography. The silicon oxide film 109 is formed within the through holes by means of the CVD method. Subsequently, the reinforcing plate is subjected to anisotropic etching such as RIE or ICP dry etching, to thus leave the silicon oxide film 109 on only the sidewalls of the through holes. As shown in Fig. 27C, the bonding pads BP are exposed.

[0283] As shown in Fig. 28A, a tungsten film is formed within the through holes as the conductor layer 108, which comes into contact with the bonding pad, by means of the CVD method using WF_6 .

[0284] As shown in Fig. 28B, the bonding pads 113 as well as the bumps 114 are formed on the surface of the reinforcing plate 701.

[0285] In this way, signal extraction electrode terminals and energization electrode terminals are formed on the reinforcing plate 701.

[0286] As shown in Fig. 28C, the anisotropic conductive film 115 (ACP) is applied over the surface of this reinforcing plate 701.

[0287] Finally, as shown in Fig. 28D, the circuit board 901 in which drive circuits are fabricated is connected to the reinforcing plate by way of the anisotropic conductive film 115. A contact layer 117 formed from a conductor layer charged in a through hole formed so as to penetrate through the circuit board and a bonding pad 118 are formed on the circuit board 901.

[0288] Accordingly, the circuit board 901 can be readily connected with a circuit board, such as a printed board, by way of the bonding pads 118. The contact layer 117 is formed while being aligned with the conductor layer 108 formed in the solid-state imaging element substrate.

[0289] Subsequently, the entirety of the wafer is diced along dicing lines DC, thereby separating the solid-state imaging devices from each other. (The drawings depict only one unit solid-state imaging device, but a plurality of solid-state imaging elements are continuously formed on one wafer.)

[0290] The solid-state imaging devices are formed very readily with superior workability.

[0291] The reinforcing plate 701 is formed from a silicon substrate on which a silicon oxide film is formed, and hence the solid-state imaging element substrate 100 can be thermally or electrically insulated.

[0292] In the embodiment, the conductor layer is formed within the through hole by means of the CVD method. However, a conductor layer can be readily charged into a contact hole having a high aspect ratio with superior workability even when a plating method, a vacuum screen printing method, or a vacuum suction method is employed.

[0293] Further, in the present embodiment, electrical connections are established on both the front and back of the circuit board having the solid-state imaging element substrate and the peripheral circuit, through use of the through holes. However, there can also be employed a method for forming contacts such that the front and back of the circuit board are electrically connected together by means of subjecting both the front and back surfaces of the circuit board to impurity diffusion.

[0294] The signal extraction electrode terminal and the energization electrode terminal can be formed on the reinforcing plate 701.

(Twenty-Fourth Embodiment)

[0295] A twenty-fourth embodiment of the present invention will now be described.

[0296] In the twenty-third embodiment, the through-hole is formed so as to penetrate through the reinforcing plate 701, and the conductor layer 111 is formed. However, in the present embodiment, the solid-state imaging element substrate is formed through use of a silicon substrate in which holes (vertical holes) have been formed beforehand. As a result, the only requirement is to form the vertical holes to a shallow depth, and hence productivity is enhanced. Further, an attempt can be made to improve a production yield. In other respects, the present embodiment is formed in the same manner as the twenty-third embodiment.

[0297] Specifically, as shown in Fig. 29A, prior to formation of solid-state imaging elements, a resist pattern is formed on the back of the silicon substrate by means of photolithography. The silicon substrate is also subjected to RIE (reactive ion etching) while the resist pattern is taken as a mask, to thus form vertical holes 118. Pads 110 made of aluminum or the like have been formed beforehand on the surface of the silicon substrate in this process, and the vertical holes 118 are then formed so as to reach the pads.

[0298] As shown in Fig. 29B, a silicon oxide film 119 is formed on the interior wall of the vertical hole by means of the CVD method.

[0299] As shown in Fig. 29C, the element region to be used for fabricating the solid-state imaging elements is formed through use of an ordinary silicon process in the same manner as in the respective embodiments.

[0300] As shown in Fig. 29D, positioning is performed by means of alignment marks formed in the outer edge of each substrate, and the sealing cover glass 200, in which the spacers 203S having a thickness of 0.1 mm are bonded to the plate-like glass substrate 201, is placed on the solid-state imaging element substrate 100 formed in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together through pressurization by means of the adhesive layer 207 of room temperature curing type. Even in this

case, processing pertaining to this process may be performed through use of surface activation room temperature bonding.

[0301] As shown in Fig. 29E, the reinforcing plate 701 is bonded to the back of this solid-state imaging element substrate 100 by means of surface activation room temperature bonding. The through holes 108 are formed in the back of the solid-state imaging element substrate so as to reach the vertical holes 119, by means of the etching method using photolithography. Even in this case, the interior walls of the through holes are desirably insulated beforehand. Further, the reinforcing plate in which the through holes have been formed beforehand may also be used.

[0302] Subsequently, processing pertaining to the processes shown in Figs. 28A through 28D, which has been described in connection with the twenty-third embodiment, is performed, whereby a solid-state imaging device, in which substrates are laminated on the circuit board having peripheral circuits formed therein, is readily formed.

[0303] As mentioned previously, in the present embodiment, the only requirement is to form the vertical holes to a shallow depth, and hence productivity is enhanced. Further, an attempt can be made to improve a manufacturing yield.

(Twenty-Fifth Embodiment)

[0304] A twenty-fifth embodiment of the present invention will now be described.

[0305] In the twenty-fourth embodiment, the contacts are formed so as to penetrate through the reinforcing plate 701, the solid-state imaging element substrate, and the circuit board, and signals are extracted from the electrodes provided on the circuit board. However, as shown in Figs. 30A and 30B, the present embodiment is characterized in that a conductor layer 120 serving as a wiring layer is formed on the sidewall and in that a signal is extracted from the electrode on the sidewall of the solid-state imaging device. In other respects, the present embodiment is formed in the same manner as the twenty-fourth embodiment.

[0306] The manufacturing processes are also performed in the same manner as in the twenty-fourth embodiment. However, the through holes are formed such that positions of the through holes correspond to the ends of the respective solid-state imaging devices. The wafer is diced along the dicing lines DC including the through holes, thereby easily forming the solid-state imaging devices in which the wiring layer is formed on the sidewall.

[0307] The conductor layer 120 to be charged into the through hole is formed from a light-shielding material such as tungsten. As a result, the solid-state imaging device is shielded from light, although not perfectly, and hence an attempt can be made to reduce the chance of a faulty operation.

[0308] If the reinforcing plate is constituted of polyimide resin, ceramic, crystallized glass, and a silicon substrate whose front and back surfaces are oxidized, as required, the reinforcing plate can perform the role of a heat-insulating substrate. Alternatively, the reinforcing plate may be formed from sealing or light-shielding material having a damp-proofing characteristic.

(Twenty-Sixth Embodiment)

[0309] A twenty-sixth embodiment of the present invention will now be described.

[0310] As shown in Fig. 28, in the twenty-third and twenty-fourth embodiments the back of the solid-state imaging element substrate 100 is stacked on a peripheral circuit board by way of the reinforcing plate. However, in the present embodiment, as shown in Fig. 31, the solid-state imaging element substrate 100 is stacked on the peripheral circuit board 901, and the reinforcing plate 701 is sequentially stacked on the back of the peripheral circuit board. In other respects, the present embodiment is formed in the same manner as the twenty-fourth or twenty-fifth embodiment.

[0311] This reinforcing plate doubles as a heatsink.

[0312] The manufacturing processes are also performed in the same manner as in the twenty-third and twenty-fourth embodiments. However, the solid-state imaging element substrate 100 and the peripheral circuit board 901 are located close to each other, and hence connection resistance is reduced correspondingly, thereby enabling high-speed operation.

[0313] A twenty-seventh embodiment of the present invention will now be described.

[0314] In the twenty-sixth embodiment, the through holes are formed in the substrate, and signals are extracted from the electrodes provided on the back of the peripheral circuit board. However, as shown in Fig. 32, the present embodiment is characterized in that the conductor layer 120 serving as a wiring layer is formed on the sidewall by way of an insulation film 121. In other respects, the present embodiment is formed in the same manner as the twenty-sixth embodiment.

[0315] Manufacturing operation is performed in substantially the same manner as in the twenty-fifth embodiment. However, a solid-state imaging device, in which a wiring pattern is formed on a sidewall, can be readily formed by means of merely setting a dicing line at a position including a contact formed in the through hole.

[0316] In this solid-state imaging device, the wiring pattern is formed on the sidewall, and hence a signal extraction terminal and a current supply terminal can also be formed on the sidewall. Needless to say, connection may be estab-

lished by means of forming pads and bumps on the back of the peripheral circuit board 901. Reference numeral 701 designates a reinforcing plate.

[0317] In the twenty-first through twenty-seventh embodiments, the sealing cover glass 200 made of low α -ray glass can be formed in the same manner as in the manufacturing methods described in connection with the first through twentieth embodiments.

(Twenty-Eighth Embodiment)

[0318] A twenty-eighth embodiment of the present embodiment will now be described.

[0319] In the twenty-third embodiment, the through holes are formed within the substrate, and signals are extracted from the electrodes provided on the back of the peripheral circuit board. As shown in Fig. 33, the present embodiment is characterized in that the conductor layer 209 is formed in the through-hole 208, which is formed in the glass substrate 201 made of low α -ray glass and in the spacer 203S having a thickness of 0.1 mm; in that a pad 217 is formed on the upper surface of the glass substrate; and in that the signal extraction terminal and the current supply terminal are formed on the surface of the glass substrate. In other respects, the present embodiment is formed in the same manner as the twenty-third embodiment shown in Figs. 27 and 28.

[0320] Processes for manufacturing the solid-state imaging device will now be shown in Figs. 34A to 34F and Figs. 35A to 35E.

[0321] In the twenty-third embodiment, the through holes are formed in the solid-state imaging element substrate 100 during the process shown in Fig. 27C, and the signal extraction terminals and the current supply terminals are formed on the back of the solid-state imaging element substrate. This method is characterized in that the spacer 203S is caused to adhere to the glass substrate 201 constituting the sealing cover glass 200; in that, in this state, the through holes 208 are formed so as to penetrate through the spacer and the glass substrate; in that conductor layers are formed in the through holes 208; and in that the signal extraction terminals and the current supply terminals are formed on the surface of the sealing cover glass.

[0322] As shown in (1) of Fig. 34A, the silicon substrate 203 from which a spacer is to be formed and which has a thickness of 30 to 120 μ m is first prepared.

[0323] Next, as shown in (2) of Fig. 34A, the glass substrate 201 to be used for constituting the sealing cover glass 200 is prepared.

[0324] As shown in Fig. 34B, the adhesive layer 202 is applied over the surface of the substrate 203.

[0325] Subsequently, as shown in Fig. 34C, the silicon substrate 203 covered with the adhesive layer 202 is caused to adhere to the surface of the glass substrate 201.

[0326] As shown in Fig. 34D, a resist pattern is formed by means of photolithography. The silicon substrate is also subjected to RIE (reactive ion etching) while the resist pattern is taken as a mask. An adhesive has been applied beforehand over the region corresponding to photodiodes; that is, an area corresponding to the light-receiving regions (designated by 40 in Fig. 1B), so as to exclude the indentation sections 205. Alternatively, the silicon substrate is subjected to removal processing through use of oxygen plasma after having undergone RIE.

[0327] As shown in Fig. 34E, a resist pattern is formed by means of photolithography. The silicon substrate is also subjected to RIE (reactive ion etching) while the resist pattern is taken as a mask, to thus form the through holes 208 so as to penetrate through the spacer 203S and the glass substrate 201.

[0328] A silicon oxide film (not shown) is formed on the interior wall of the spacer formed from silicon by means of at least CVD, as required.

[0329] When the spacer is formed from an insulator, such as glass or resin, this process becomes unnecessary. A light-shielding film may be formed on the interior wall or exterior wall of the spacer.

[0330] As shown in Fig. 35A, the conductor layer 209 is formed on the insulated interior wall of the through hole by means of vacuum screen printing or metal plating using conductive paste, such as silver paste or copper paste, to thus form a through contact region which penetrates through the spacer 203S and the glass substrate 201.

[0331] As shown in Fig. 35B, gold bonding pads 210, 211 and the bumps 212 are formed on the front and back of the glass substrate with the spacer so as to connect with the through contact region. A thin gold film is formed on the front and back of the glass substrate at the time of formation of a film, and the substrate is patterned by means of the etching method using photolithography. Screen printing or selective plating can also be applied to the patterning.

[0332] As shown in Fig. 35C, an anisotropic conductive resin film 213 is applied over the bump and the pad.

[0333] As shown in Fig. 35D, the solid-state imaging element substrate 100 in which the reinforcing plate 701 is formed is prepared in the same manner as in the twenty-third embodiment (see Fig. 27A).

[0334] As shown in Fig. 35E, positioning is performed by means of the alignment marks formed in the outer edges of the respective substrates, and the sealing cover glass 200, in which the spacers 203S are bonded to the flat-plate-like glass substrate 201, is placed on the solid-state imaging element substrate 100 formed in the manner mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 200 are integrated together by

means of the anisotropic conductive film 213.

[0335] Subsequently, the entirety of the wafer is diced along the dicing lines DC, to thereby separate the solid-state imaging devices apart from each other.

[0336] In this way, the solid-state imaging device can be formed very easily with superior operability, wherein the contact region, such as bonding pads, is formed on the sealing cover glass.

(Twenty-Ninth Embodiment)

[0337] A twenty-ninth embodiment of the present invention will now be described.

[0338] The twenty-eighth embodiment has described the solid-state imaging device, wherein the through holes that penetrate through the glass substrate made of low α -ray glass and the spacer having a thickness of 0.1 mm are formed, and wherein the contact region, such as bonding pads, is formed on the sealing cover glass. However, thirtieth to thirty-third embodiments will describe modifications of this embodiment.

[0339] The present embodiment is characterized by forming the through holes in the spacer. As shown in Fig. 36A, the glass substrate 201 is prepared.

[0340] As shown in Fig. 36B, photocuring resin is formed on the surface of the glass substrate 201 by means of an optical molding method, to thus form a spacer 213.

[0341] Subsequently, as shown in Fig. 36C, the through holes 208 are formed by means of the etching method using photolithography.

[0342] As mentioned above, the sealing cover glass which has the spacer and in which the through holes are formed can be readily obtained.

[0343] Processing pertaining to the mounting processes shown in Figs. 35A to 35E is performed in the same manner as described in connection with the twenty-eighth embodiment. The sealing cover glass is caused to adhere to the solid-state imaging element substrate, and the wafer is diced. As a result, solid-state imaging devices shown in Fig. 35E can be formed.

[0344] By means of this method, the spacer is formed readily. Although the photocuring resin has been employed in the embodiment, an adhesive itself may be employed. The glass substrate and the spacer are formed integrally, thereby diminishing warpage or distortion and facilitating manufacturing operation.

(Thirtieth Embodiment)

[0345] A thirtieth embodiment of the present invention will now be described.

[0346] In the twenty-eighth embodiment, the silicon substrate for use in forming a spacer is caused to adhere to the glass substrate made of low α -ray glass, and the wafer is patterned. However, in the present embodiment, the glass substrate is etched during a single etching process, and indentation sections and through holes may be formed simultaneously. In other respects, the present embodiment is formed in the same manner as in the twenty-eighth embodiment.

[0347] As shown in Fig. 37A, the glass substrate 201 is prepared in the present embodiment.

[0348] As shown in Fig. 37B, the resist pattern is formed on the front and back of the glass substrate 201. Openings are provided in the areas on both front and back surfaces of the glass substrate, where the through holes are to be formed, and openings are provided only in the back of the indentation sections 205 and the back of the area where the slice grooves 204 are to be formed, as required.

[0349] As shown in Fig. 37C, both surfaces of the glass substrate are etched while the resist patterns provided on both sides are taken as masks, to thus simultaneously form the indentation sections 205, the slice grooves (not shown), and the through holes 208.

[0350] As mentioned above, the spacer having a thickness of 0.1 mm is formed integrally, and the sealing cover glass having the through holes formed therein can be obtained.

[0351] Subsequently, processing pertaining to the mounting processes shown in Figs. 35A through 35E in the same manner as described in connection with the twenty-eighth embodiment. The sealing cover glass is caused to adhere to the solid-state imaging element substrate, and the wafer is diced. As a result, the solid-state imaging device shown in Fig. 35E can be obtained.

[0352] The glass substrate and the spacer are formed integrally, whereby warpage and distortion can be diminished, and manufacturing operation is also facilitated.

(Thirty-First Embodiment)

[0353] A thirty-first embodiment of the present invention will now be described.

[0354] In the twenty-eighth embodiment, the silicon substrate for use in forming a spacer is caused to adhere to the

glass substrate made of low α -ray glass, and the wafer is patterned. However, in the present embodiment, the spacer 203S in which the pattern has already been formed and which has a thickness of 0.1 mm is caused to adhere to the glass substrate 201, and the through holes are finally formed during the etching process. In other respects, the present embodiment is formed in the same manner as the twenty-eighth embodiment.

[0355] In the present embodiment, as shown in (1) of Fig. 38A, the glass substrate 201 is prepared.

[0356] As shown in (2) of Fig. 38A, the silicon substrate 203 for use in forming a spacer is prepared.

[0357] As shown in Fig. 38B, the silicon substrate 203 is processed by means of the etching method using photolithography, thereby producing the spacer 203S.

[0358] As shown in Fig. 38C, the adhesive 202 is applied over the surface of the thus-patterned spacer.

[0359] As shown in Fig. 38D, the spacer 203S is caused to adhere to the glass substrate 201.

[0360] As shown in Fig. 38E, the through holes 208 are formed by means of the etching method using photolithography.

[0361] As mentioned above, the spacer is caused to adhere to the glass substrate readily, and the sealing cover glass having the through holes formed therein can be readily obtained.

[0362] A silicon oxide film (not shown) is formed on the interior wall of the spacer formed from silicon by means of at least CVD, as required.

[0363] When the spacer is formed from an insulator, such as glass or resin, this process becomes unnecessary. A light-shielding film may be formed on the interior wall or exterior wall of the spacer. Subsequently, processing pertaining to the mounting processes shown in Figs. 35A through 35E is performed in the same manner as described in connection with the twenty-eighth embodiment. The sealing cover glass is caused to adhere to the solid-state imaging element substrate, and the wafer is diced. As a result, the solid-state imaging device shown in Fig. 35E can be obtained.

[0364] When the spacer is caused to adhere to the glass substrate, adhesion may be performed through use of UV-radiation curing resin, thermosetting resin, a combination thereof, or application of a semi-curing-type adhesive, within a range in which there does not arise warpage in the wafer due to a difference in thermal expansion coefficient, a reduction in reliability stemming from application of thermal stress on the solid-state imaging elements, or a failure in fastening of a wafer in a subsequent process. At the time of formation of the adhesive, supply of the adhesive through use of a dispenser, screen printing, or stamping transfer can be selected, as required.

[0365] As shown in Fig. 38C, a light-shielding film 215 may have been formed beforehand on the interior walls of indentation sections of the spacer by means of a method for sputtering a tungsten film.

[0366] As a result, a superior image capturing characteristic can be obtained without involvement of provision of an additional light-shielding film.

(Thirty-Second Embodiment)

[0367] A thirty-second embodiment of the present invention will now be described.

[0368] The twenty-eighth embodiment has described a case where the silicon substrate for use in forming a spacer is caused to adhere to the glass substrate made of low α -ray glass; where the glass substrate is patterned; and where the through holes penetrating through the glass substrate and the spacer are finally formed by means of etching. In the present embodiment, as shown in Figs. 39A to 39F, the geometry of the silicon substrate is processed by means of etching. The spacer 203S which is shown in Fig. 39E and which has the through hole 208a formed therein and a thickness of 0.1 mm is aligned with the glass substrate 201 which is shown in Fig. 39C and which has through holes 208b formed therein through use of alignment marks on the wafer scale. The spacer 203S and the glass substrate 201 are bonded together through use of the adhesive layer 202. In other respects, the present embodiment is formed in the same manner as the twenty-eighth embodiment.

[0369] Even in this case, the light-shielding film (215) can be formed on an interior wall of the glass substrate facing the indentation section of the spacer.

[0370] By means of this method, the through-holes are formed individually, and the spacer and the glass substrate are bonded together. Therefore, alignment is required, but an aspect ratio of about one-half is required; and hence formation of the through holes becomes easy. Subsequently, processing pertaining to the mounting processes shown in Figs. 35A through 35E is performed in the same manner as described in connection with the twenty-eighth embodiment. The sealing cover glass is caused to adhere to the solid-state imaging element substrate, and the wafer is diced. As a result, the solid-state imaging device shown in Fig. 35E can be obtained.

(Thirty-Third Embodiment)

[0371] A thirty-third embodiment of the present invention will now be described. In the twenty-eighth embodiment, the silicon substrate for use in forming a spacer is caused to adhere to the glass substrate made of low α -ray glass, the conductor layer 209 has been formed in the through holes that penetrate through the glass substrate remaining in

the etching process, and the spacer has a thickness of 0.1 mm. Subsequently, the solid-state imaging element substrate 100 is caused to adhere to the silicon substrate. However, as shown in Figs. 40A through 40D, the present embodiment is characterized in that the glass substrate 200 with the spacer in which the through hole 208 formed in the twenty-eighth through thirty-second embodiments is formed is aligned on the wafer scale and bonded with and to the solid-state imaging element substrate 100 having the reinforcing plate 701 affixed to the back thereof; and that, subsequently, the conductor layer 209 is formed within the through hole 208. Further, the bonding pads 210 are formed so as to connect with the conductor layer 209. In other respects, the present embodiment is formed in the same manner as the twenty-eighth embodiment.

[0372] Here, at the time of embedment of the conductor layer 209, the embedment can be readily realized through use of vacuum screen printing using conductive paste such as copper paste or metal plating.

(Thirty-Fourth Embodiment)

[0373] A thirty-fourth embodiment of the present invention will now be described.

[0374] In the first through thirty-third embodiments, the sealing cover glass made of a plate-like member, which is formed from low α -ray glass, is used as the light-transmission member. However, an attempt can be made to further miniaturize the solid-state imaging device by means of imparting an imaging function to the sealing cover glass to constitute an optical member.

[0375] As shown in Fig. 41, the solid-state imaging device is characterized in that a sealing cover glass 220 with a lens array is used in place of the sealing cover glass 200 described in connection with the twenty-eighth embodiment through the thirty-third embodiment.

[0376] The sealing cover glass 220 is formed by means of the molding method or the etching method.

[0377] In other respects, the present embodiment is formed in the same manner as the twenty-eighth embodiment.

[0378] As shown in Fig. 33, in the twenty-eighth embodiment, the conductor layer is formed in the through holes 208, which are formed in the glass substrate 201 and the spacer 203S, and the pads 210 are formed on the upper surface of the glass substrate. The signal extraction terminals and the current supply terminals are formed on the surface of the sealing cover glass. However, in the present embodiment, the bonding pads BP are connected to external connection terminals in some unillustrated regions. In other respects, the present embodiment is formed in the same manner as the twenty-eighth embodiment shown in Figs. 33 and 34.

[0379] Processes for manufacturing the solid-state imaging device are shown in Figs. 42A to 42D and Figs. 43A to 43C.

[0380] Specifically, the manufacturing processes differ from those described in connection with the twenty-eighth embodiment in that the sealing cover glass 220 with a lens array is used in place of the sealing cover glass 200 described in connection with the twenty-eighth through thirty-third embodiments.

[0381] In the thirty-third embodiment, the spacer 203S having a thickness of 0.1 mm is affixed to the glass substrate 201 constituting the sealing cover glass 200. In this state, the through holes 208 are formed so as to penetrate through the spacer and the glass substrate. The conductor layer is formed in the through holes 208, and the signal extraction terminals and the current supply terminals are formed on the surface of the surface of the sealing cover glass. In this embodiment, the same configuration may be adopted.

[0382] The adhesive layer 207 of room temperature curing type is formed on the surface of the spacer 203S of the sealing cover glass 220 with the lens array which is formed during the processes shown in Figs. 42A to 42D (shown in Fig. 43A).

[0383] As shown in Fig. 43B, the solid-state imaging element substrate 100 in which the reinforcing plate 701 is formed is prepared in the same manner as in the twenty-eighth embodiment.

[0384] Positioning is performed by means of the alignment marks formed in the outer edges of the respective substrates as shown in Fig. 43C. The cover glass 220 with the lens array, to which a spacer 203S is bonded, is placed on the solid-state imaging element substrate 100 formed in the manner as mentioned previously. The solid-state imaging element substrate 100 and the sealing cover glass 220 are integrated together by means of the adhesive layer 207 of room temperature curing type.

[0385] Modifications of the processes for manufacturing the sealing cover glass 220 with the lens array will be described in connection with thirty-fifth through thirty-eighth embodiments.

(Thirty-Fifth Embodiment)

[0386] A thirty-fifth embodiment of the present invention will now be described.

[0387] As shown in Figs. 44A and 44B, the present embodiment is characterized in that the sealing cover glass 220 with a lens array made of low α -ray glass is prepared and that an indentation section 225 is formed in the back of the cover glass by means of etching, to thus integrally form the spacer 223S having a thickness of 0.1 mm. In other respects,

the present embodiment is formed in the same manner as in the previous embodiments.

[0388] The sealing cover glass can be readily formed with superior workability by means of this configuration. Since the spacer is formed integrally, the highly reliable sealing cover glass 220 with the lens array can be obtained without occurrence of distortion.

(Thirty-Sixth Embodiment)

[0389] A thirty-sixth embodiment of the present invention will now be described.

[0390] As shown in Fig. 45A, the glass substrate 220 with the lens array is prepared.

[0391] As shown in Fig. 45B, photocuring resin is formed on the surface of the glass substrate 220 with the lens array by means of an optical molding method, to thus form the spacer 223 having a thickness of 0.1 mm. Thus, the sealing cover having the through holes formed therein and the spacer can be readily obtained. Subsequently, processing pertaining to the mounting processes shown in Figs. 43A through 43C are performed in the same manner as described in connection with the thirty-fourth embodiment. The sealing cover glass is caused to adhere to the solid-state imaging element substrate, and the wafer is diced. As a result, the solid-state imaging device shown in Fig. 43C can be obtained.

(Thirty-Seventh Embodiment)

[0392] A thirty-seventh embodiment of the present invention will now be described.

[0393] In the thirty-fourth embodiment, the silicon substrate is caused to adhere to the glass substrate which is made of low α -ray glass and has a lens array, and the silicon substrate is patterned. As shown in Figs. 46A to 46D, the spacer 203S which has been formed by means of the etching method and has a thickness of 0.1 mm may be caused to adhere to the sealing cover glass 220 with a lens array. Even in this case, the cover glass is caused to adhere to the solid-state imaging element during the mounting process in the same manner as in the thirty-sixth embodiment, and the wafer is subjected to dicing, whereby the solid-state imaging device can be obtained.

(Thirty-Eighth Embodiment)

[0394] A thirty-eighth embodiment of the present invention will now be described.

[0395] As shown in Fig. 47, the sealing cover glass 220 with a lens array, the spacer 203S having a thickness of 0.1 mm, and the solid-state imaging element substrate 100 having the reinforcing plate 701 may be fixed together simultaneously.

(Thirty-Ninth Embodiment)

[0396] A thirty-ninth embodiment of the present invention will now be described.

[0397] As shown in Figs. 48A through 48D, the sealing cover glass 220 with the lens array made of low α -ray glass can also be applied to the solid-state imaging device in which the peripheral circuit board 901 shown in Figs. 28A through 28D in the twenty-third embodiment is stacked on the substrate by way of the anisotropic conductive film 115. In other respects, the present embodiment is formed in the same manner as in the previously-described embodiments.

[0398] Even at the time of connection of the peripheral circuit board 901, diffusion bonding using ultrasonic waves, solder bonding, and eutectic bonding based on thermocompression can also be effectively employed in place of the anisotropic conductive film. Moreover, the peripheral circuit board may be under-filled with resin.

[0399] The sealing cover glass 220 with the lens array may also be used in place of the sealing cover glass 200 made of a plate-like material.

(Fortieth Embodiment)

[0400] A fortieth embodiment of the present invention will now be described.

[0401] As shown in Fig. 49, the solid-state imaging element substrate 100, the peripheral circuit board 901, and the reinforcing plate 701 may be stacked in this sequence in the same manner as shown in Fig. 31 in connection with the twenty-sixth embodiment. In other respects, the present embodiment is formed in the same manner as in the previously-described embodiments.

(Forty-First Embodiment)

[0402] A forty-first embodiment of the present invention will now be described.

[0403] As shown in Fig. 50, a spacer having a wiring pattern 221 provided on a sidewall thereof and a thickness of 0.1 mm is also effective.

[0404] Manufacture of the spacer is the same as in the twenty-seventh embodiment. Through holes are formed in the spacer, and the conductor layer is formed in the through holes. After the solid-state imaging substrate and the cover glass 220 with a lens have been affixed together, the wafer is sliced along the dicing lines including the through holes, thereby readily enabling wiring on the sidewall. In other respects, the present embodiment is formed in the same manner as in the previously-described embodiments.

[0405] The embodiments have described the method for bonding the glass substrate constituting the sealing cover glass to the spacer and bonding the solid-state imaging element substrate to the sealing cover glass through use of the adhesive layer. When the spacer and the surface of the solid-state imaging element substrate, both pertaining to all the embodiments, are made of Si, metal, or an inorganic compound, the spacer and the solid-state imaging element substrate may also be bonded together without use of an adhesive, by means of surface activation room temperature bonding, as required. When the cover glass is made of Pyrex glass and the spacer is made of Si, anode bonding is also possible. When the adhesive layer is used, a thermosetting adhesive or a thermosetting/UV curing combined adhesive can be employed as the adhesive layer in place of the UV adhesive, within the range in which there does not arise warpage in the wafer due to a difference in thermal expansion coefficient, a reduction in reliability stemming from application of thermal stress on the solid-state imaging elements, or a failure in fastening of a wafer in a subsequent process.

[0406] When the semi-curing type adhesive is used, the adhesive is applied in a liquid status. The adhesive is semi-cured, and positioning is performed. As a result, a modification can be made during positioning operation, and hence a solid-state imaging device which has been aligned with high accuracy can be formed.

[0407] Although having been described in connection with the first embodiment, a material of the spacer described in connection with all the embodiments can be selected from any of a 42 alloy, metal, glass, photosensitive polyimide, and polycarbonate resin, as well as a silicon substrate, as required.

[0408] When the solid-state imaging element substrate and the sealing cover glass are bonded together through use of an adhesive layer, a sump is formed, thereby preventing outflow of a melted adhesive layer. The same also applies to a junction between the spacer and the solid-state imaging element substrate or a junction between the spacer and the sealing cover glass. As can be seen in Figs. 51A through 51F, which show example shapes of the junction end of the spacer, indentation sections or protrusion sections may be formed in the junction, thereby preventing outflow of the melted adhesive layer.

[0409] Moreover, with a view toward rendering sturdy the bonding between the solid-state imaging element substrate and the sealing cover glass and preventing deterioration of the solid-state imaging elements, the junction between the glass substrate 200 including the sealing cover glass 201 and the spacer 203S and the junction between the spacer and the solid-state imaging element substrate 100 may be sealed with sealing resin M, as shown in Fig. 52, thereby preventing intrusion of moisture and achieving high reliability.

[0410] Epoxy-based sealing resin, oxetane-based sealing resin, silicon-based sealing resin, and acrylic sealing resin are suitable as sealing resin. Any resin may be adopted, so long as it enables formation of a desired sealing region, prevention of intrusion of moisture, and acquisition of high reliability.

[0411] At the time of formation, sealing resin is supplied to the region exclusive of the bonding pads BP (electrode pads) through use of a jig, such as a dispenser. After the sealing resin has been cured, the jig is removed, thereby realizing resin sealing without overturning the bonding pads. As in the case of the previously-described adhesive, sealing resin which can be cured at 80°C or less is desirable. Use of photocuring resin or room temperature curing type resin as resin is desirable. When photocuring resin is used, a jig is desirably constituted of a light-transmission member.

[0412] In the previous embodiments, separation of the substrate having the slice grooves formed therein into pieces is performed by means of carrying out CMP to the positions of the slice grooves. However, grinding, polishing, or overall etching can also be used.

[0413] In the embodiments, when the reinforcing plate (701) is used, the reinforcing plate is constituted of polyimide resin, ceramic, crystallized glass, or a silicon substrate whose front and back surfaces are oxidized, as required. As a result, the role of a heat insulating substrate can be imparted to the reinforcing plate. Alternatively, the reinforcing plate may be made of light-shielding material.

[0414] In the embodiments, when the glass substrate and the spacer must be affixed together, affixing operation may be performed through use of UV-radiation curing resin, thermosetting resin, a combination thereof, or application of a semi-curing-type adhesive, within a range in which there does not arise warpage in the wafer due to a difference in thermal expansion coefficient, a decrease in reliability as a result of application of thermal stress to the solid-state imaging elements, or a failure in wafer bonding to be performed in a subsequent process.

[0415] At the time of formation of the adhesive, supply of the adhesive through use of a dispenser, screenprinting, or stamping transfer can be selected, as required.

[0416] In addition, the examples described in connection with the embodiments can be mutually modified within a range in which the modifications are applicable to all the embodiments.

[0417] As has been described, according to the solid-state imaging device of the present invention, the low α -ray glass is used as the light-transmission member, and hence a highly reliable solid-state imaging device with little image noise can be provided.

[0418] According to the method for manufacturing a solid-state imaging device of the present invention, the low α -ray glass is used as the light-transmission member, and positioning is performed on the wafer scale. The elements are mounted in a collective manner, including formation of external extraction electrode terminals, thereby integrating the elements. Subsequently, the wafer is separated, for each solid-state imaging element. Accordingly, a highly-reliable solid-state imaging device which is easy to manufacture can be formed.

[0419] The solid-state imaging device of the present invention is applicable to a digital camera.

Claims

1. A solid-state imaging device, comprising:

a semiconductor substrate (101) having a first surface;
a solid-state imaging element (102) in the first surface of semiconductor substrate, the solid-state imaging element comprising a light-receiving region;
a light-transmission member (201) having a second surface and a third surface, the second surface being opposite to the third surface, wherein the light-transmission member and the first surface of the semiconductor substrate define a gap (C) between the second surface of the light-transmission member and an outer surface of the light-receiving region; and
an external connection terminal (BP) connected to the solid-state imaging element,

wherein the light-transmission member comprises low α -ray glass.

2. The solid-state imaging device according to claim 1, wherein the light-transmission member (201) has an α -ray threshold limit value of 0.002 or less (DPH/cm²).

3. The solid-state imaging device according to claim 1 or 2, wherein the distance between the outer surface of the light-receiving region and the third surface of the light-transmission member (201) is 0.5 mm or more.

4. The solid-state imaging device according to claim 3, wherein the distance between the outer surface of the light-receiving region and the third surface of the light-transmission member (201) does not exceed 1.5 mm.

5. The solid-state imaging device according to any preceding claim, further comprising a spacer (203 S) between the second surface of the light-transmission member (201) and the first surface of the semiconductor substrate (101) so that a distance between the outer surface of the light-receiving region and the third surface of the light-transmission member is set to be a predetermined value.

6. The solid-state imaging device according to claim 5, wherein the spacer (203 S) comprises silicon.

7. The solid-state imaging device according to claim 5 or 6, wherein the spacer (203 S) is connected to at least one of the first surface of the semiconductor substrate (101) and the second surface of the light-transmission member (201) via a temperature-curing type adhesive.

8. The solid-state imaging device according to claim 5, 6 or 7, wherein the spacer (203S) is connected to at least one of the first surface of the semiconductor substrate (101) and the second surface of the light-transmission member (201) via a photo-curing type adhesive.

9. The solid-state imaging device according to any of claims 5 to 8, wherein the width of the spacer (203S) is 100 to 500 μ m.

10. A method for manufacturing a solid-state imaging device, comprising the steps of:

forming a plurality of solid-state imaging elements (102) in a surface of a semiconductor substrate (101), each

of the solid-state imaging elements comprising a light-receiving region;
 connecting a light-transmission member (201) that comprises low α -ray glass to the surface of the semiconductor substrate, so as to define a gap (C) between the light-transmission member and an outer surface of the light-receiving region, to form an integrated member;
 5 forming external connection terminals (BP) corresponding to the solid-state imaging elements, to form an integrated member with the external connection terminals; and
 separating the integrated member with the external connection terminals, for each of the solid-state imaging elements.

10 11. The method for manufacturing a solid-state imaging device according to claim 10, wherein the connecting step is performed at a temperature that does not exceed 80°C.

12. The method for manufacturing a solid-state imaging device according to claim 11, wherein the connecting step is a step using a room temperature-curing type adhesive.

15 13. The method for manufacturing a solid-state imaging device according to claim 11, wherein the connecting step is a step using a photo-curing type adhesive.

FIG. 1A

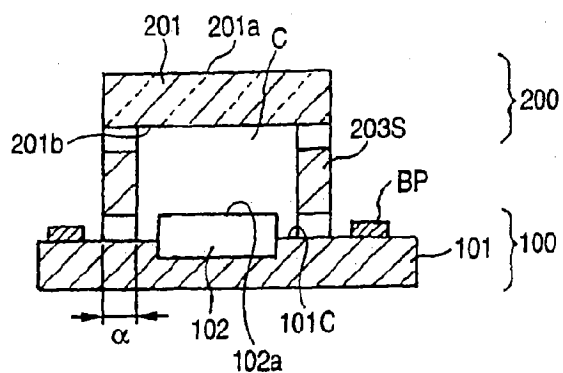


FIG. 1B

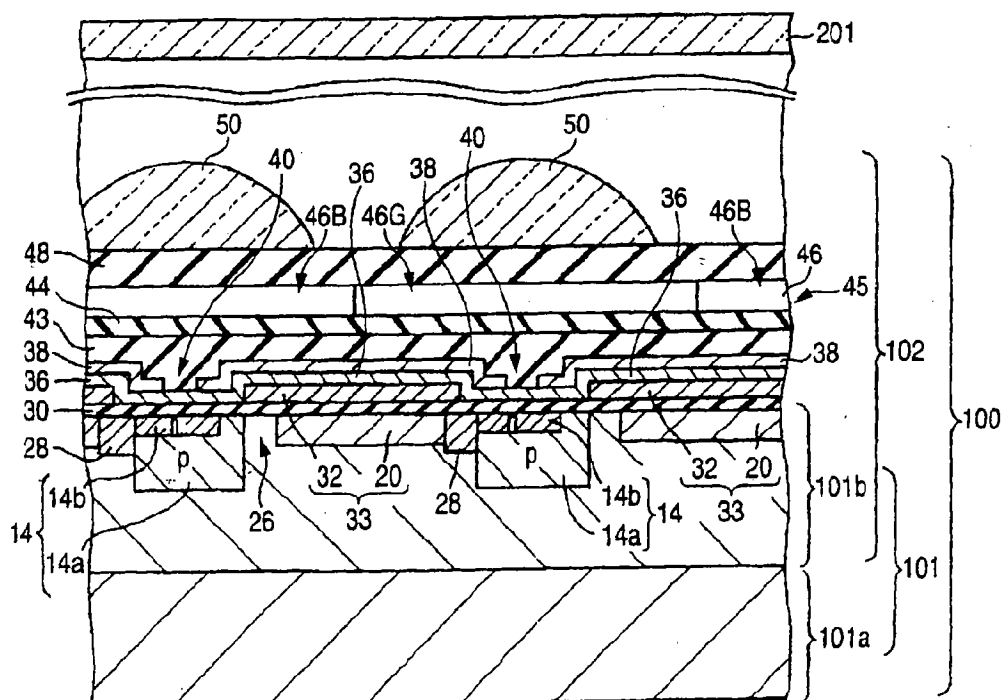


FIG. 2A

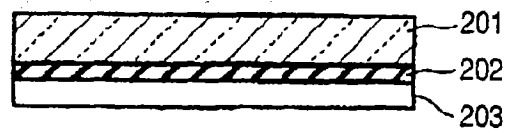


FIG. 2B

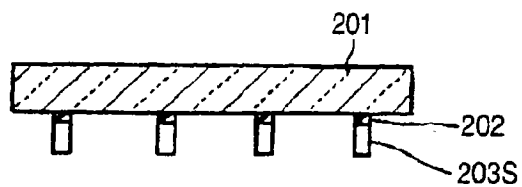


FIG. 2C

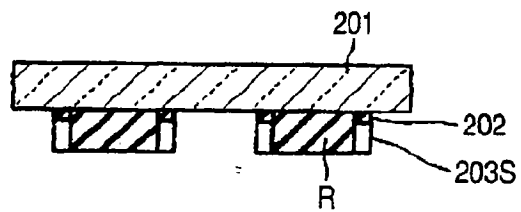


FIG. 2D

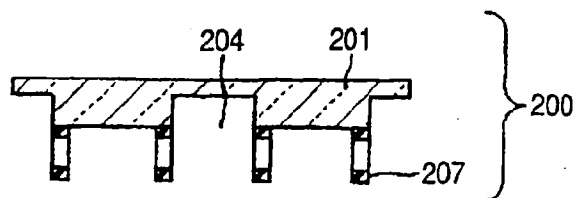


FIG. 3A

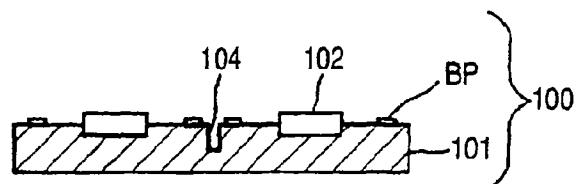


FIG. 3B

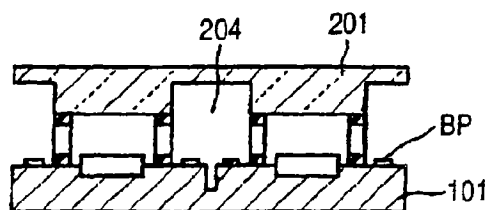


FIG. 3C

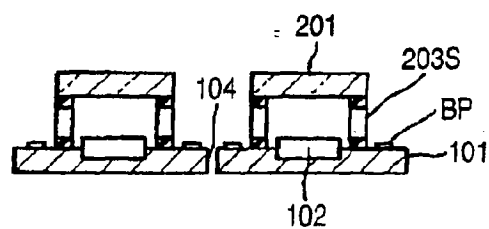


FIG. 4A

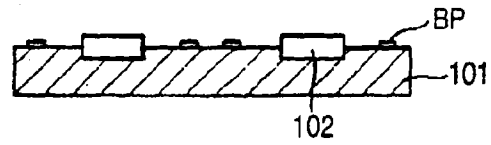


FIG. 4B

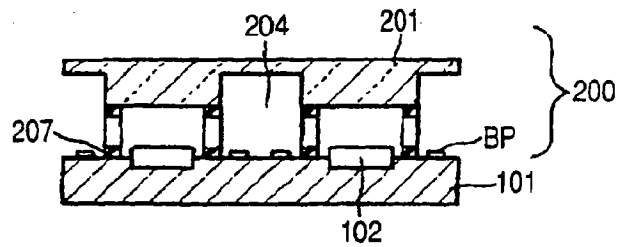


FIG. 4C

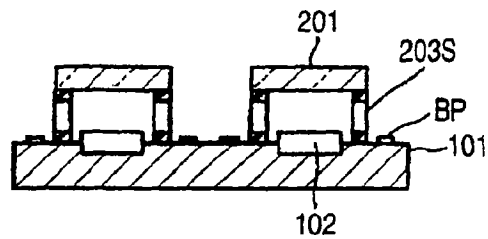


FIG. 4D

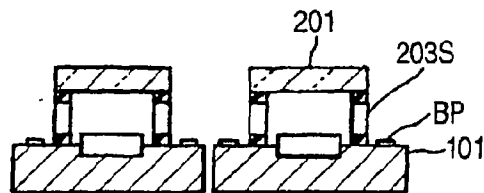


FIG. 5A

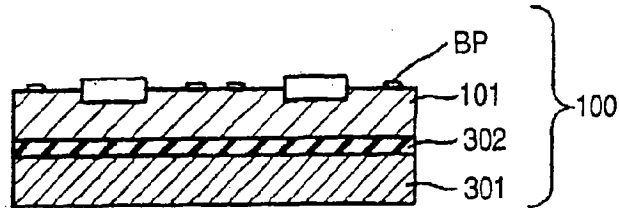


FIG. 5B

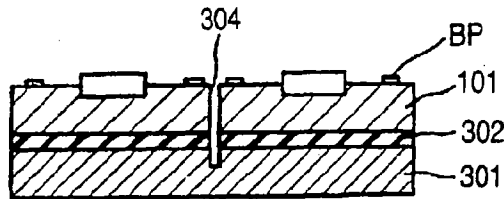


FIG. 5C

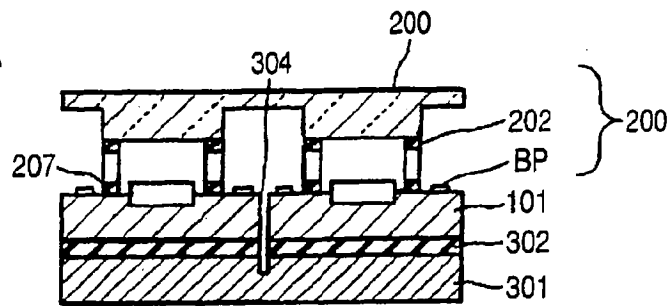


FIG. 5D

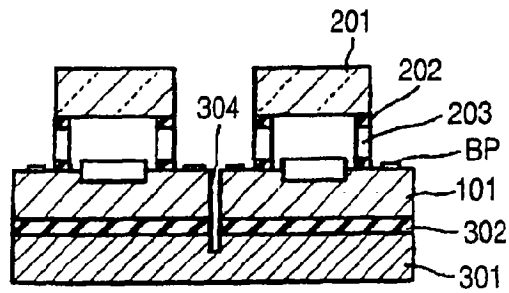


FIG. 5E

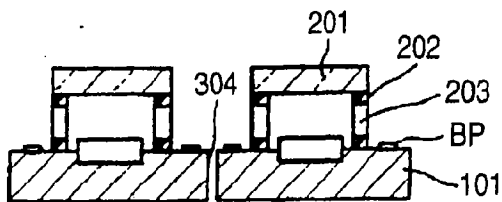


FIG. 6A

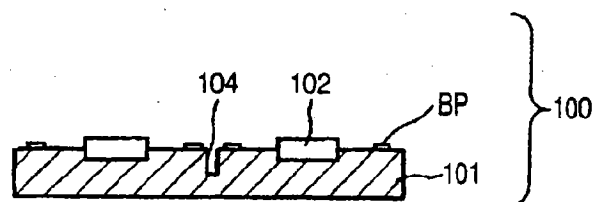


FIG. 6B

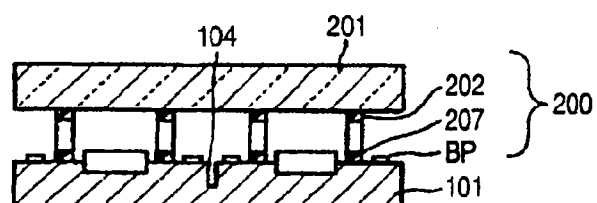


FIG. 6C

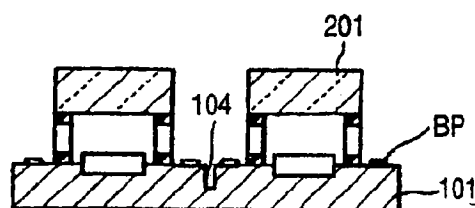


FIG. 6D

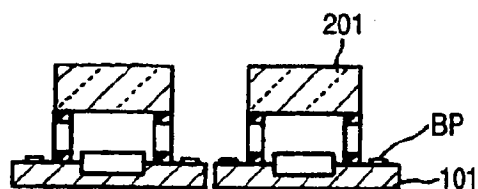


FIG. 7A

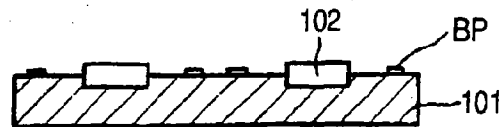


FIG. 7B

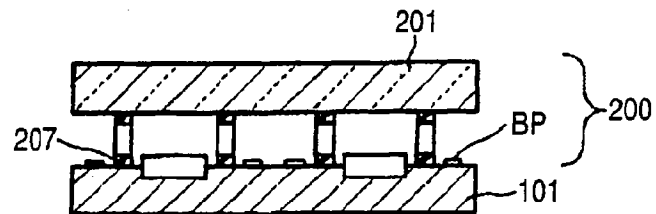


FIG. 7C

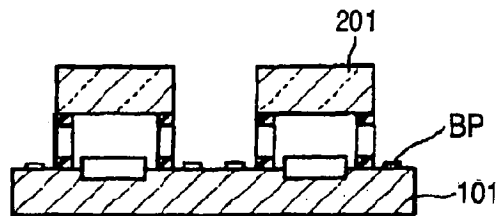


FIG. 7D

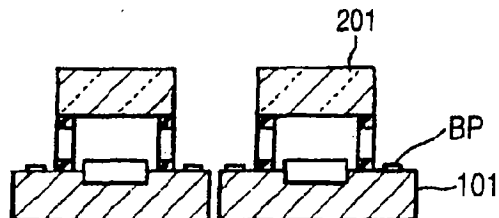


FIG. 8A

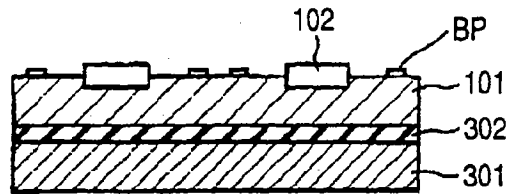


FIG. 8B

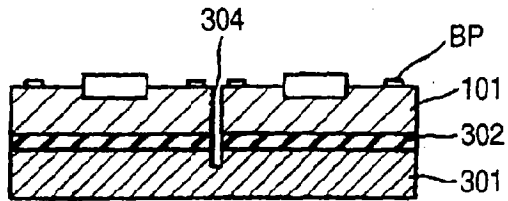


FIG. 8C

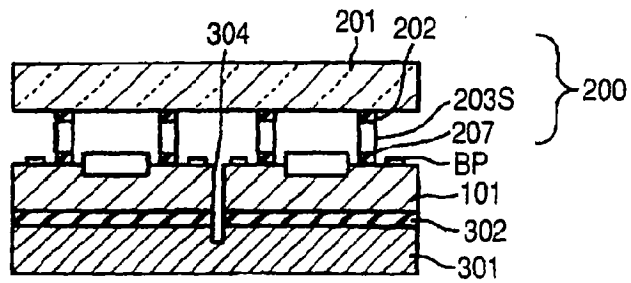


FIG. 8D

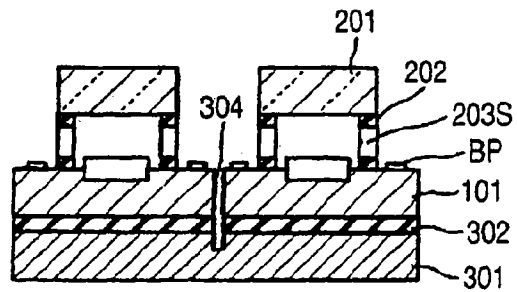


FIG. 8E

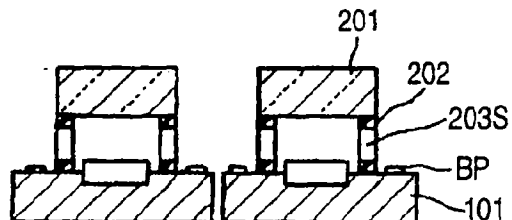


FIG. 9A

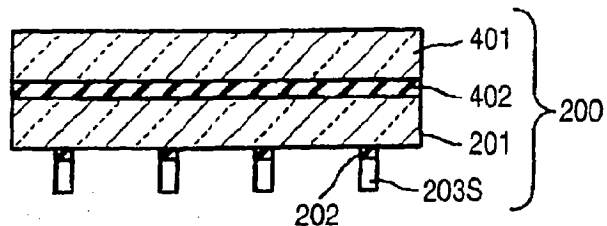


FIG. 9B

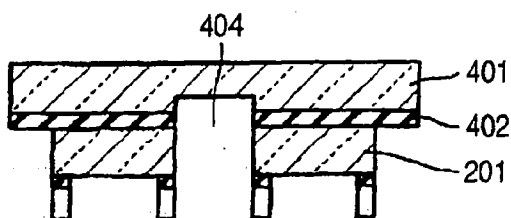


FIG. 9C

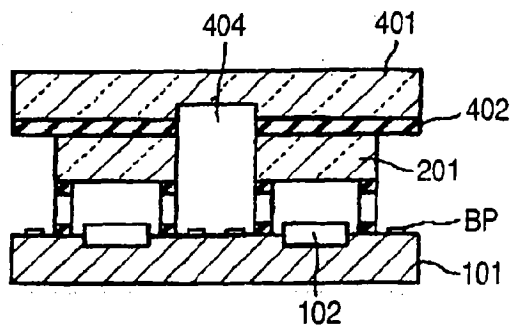


FIG. 9D

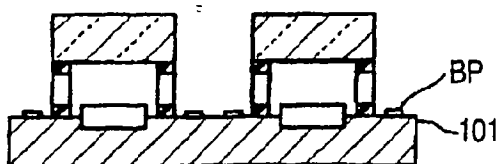


FIG. 9E

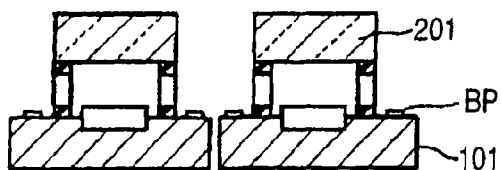


FIG. 10A

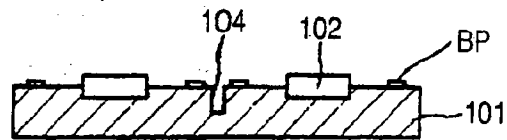


FIG. 10B

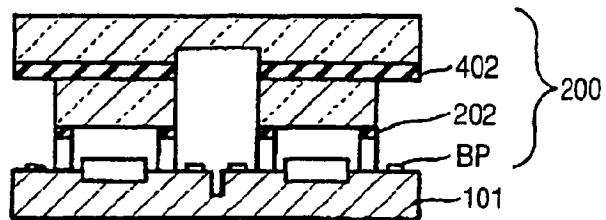


FIG. 10C

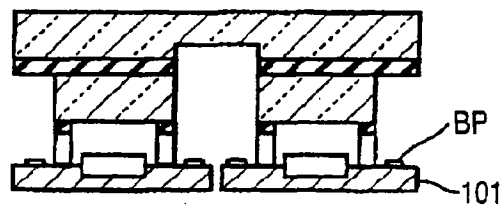


FIG. 10D

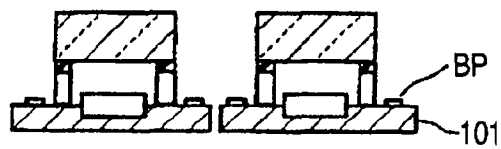


FIG. 11A

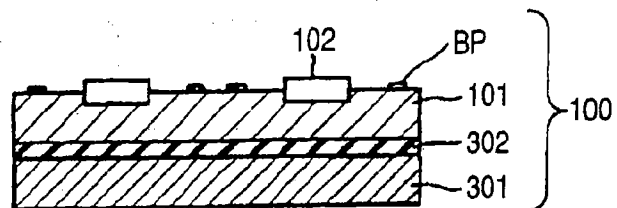


FIG. 11B

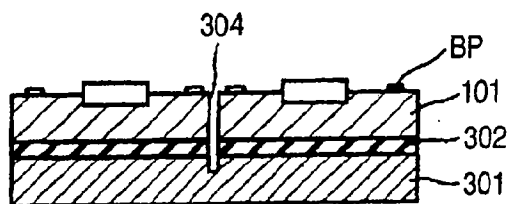


FIG. 11C

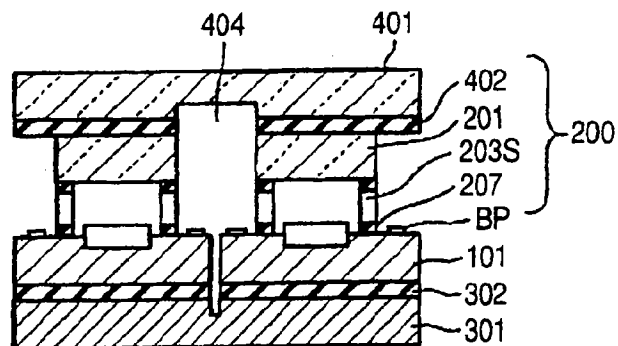


FIG. 11D

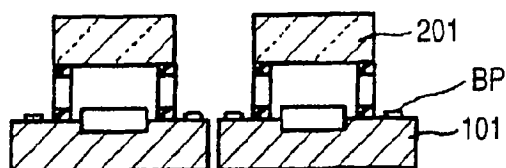


FIG. 12A

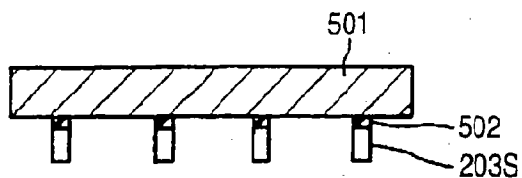


FIG. 12B

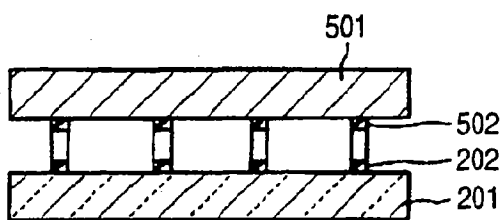


FIG. 13

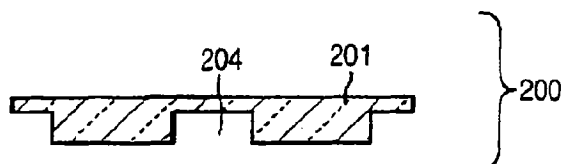


FIG. 14A



FIG. 14B

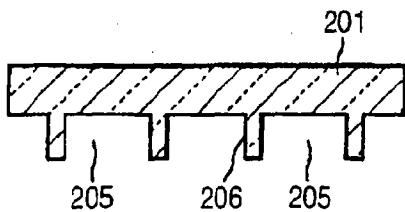


FIG. 15A

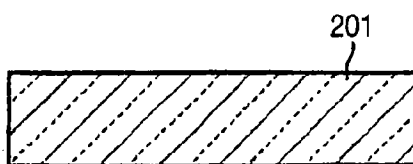


FIG. 15B

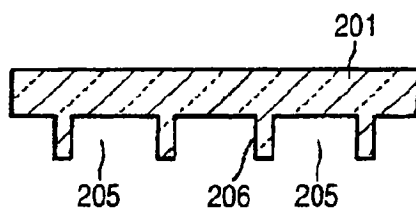


FIG. 15C

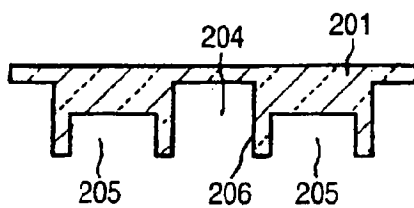


FIG. 16A

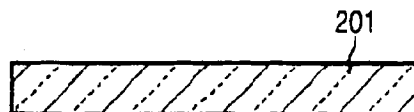


FIG. 16B

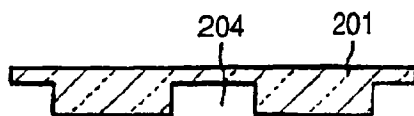


FIG. 16C

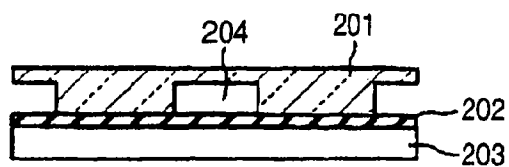


FIG. 16D

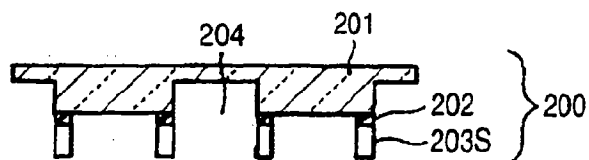


FIG. 17A

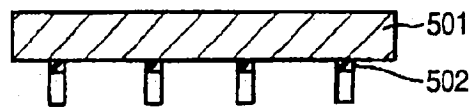


FIG. 17B

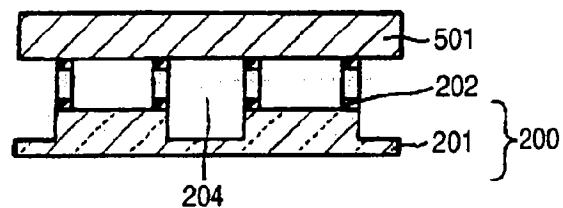


FIG. 17C

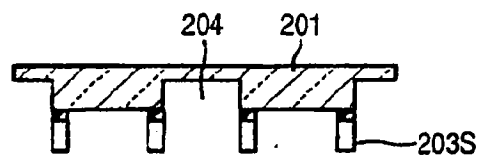


FIG. 18

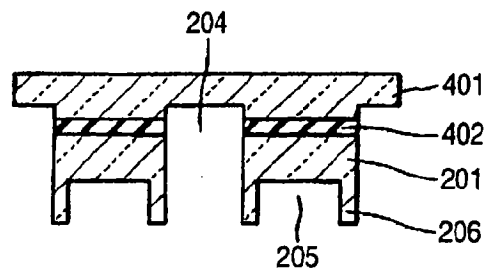


FIG. 19A

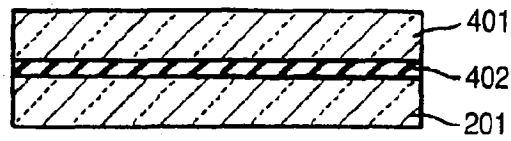


FIG. 19B

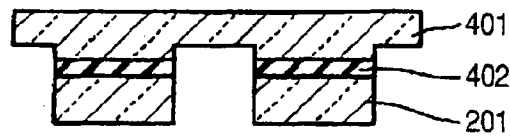


FIG. 19C

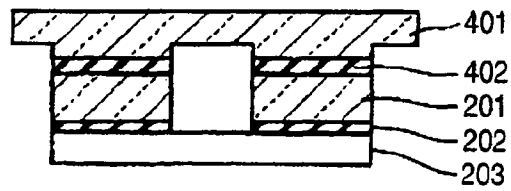


FIG. 19D

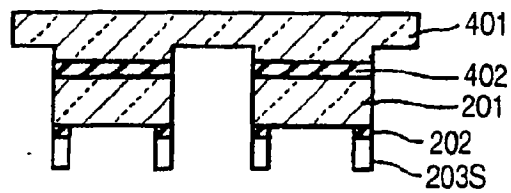


FIG. 20A

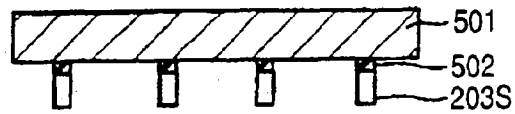


FIG. 20B

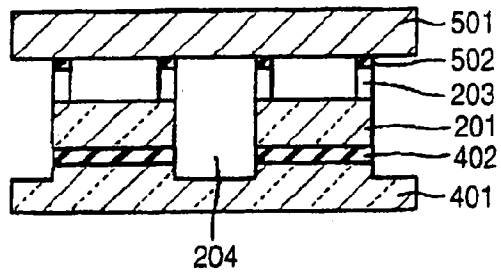


FIG. 20C

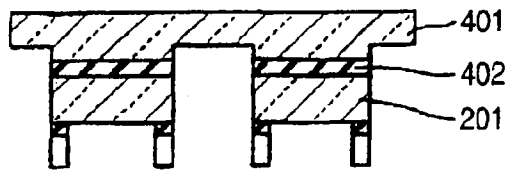


FIG. 21A

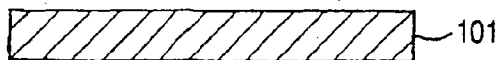


FIG. 21B



FIG. 21C

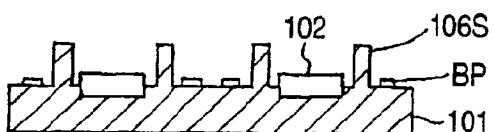


FIG. 21D

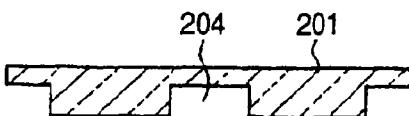


FIG. 21E

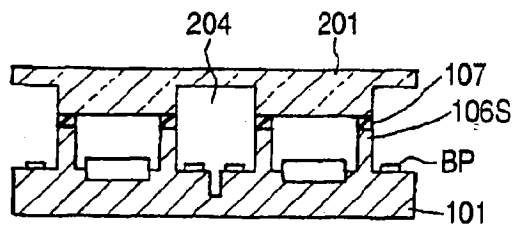


FIG. 21F

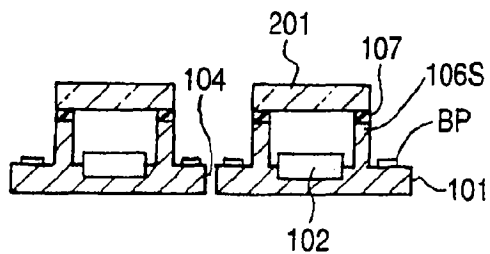


FIG. 22A

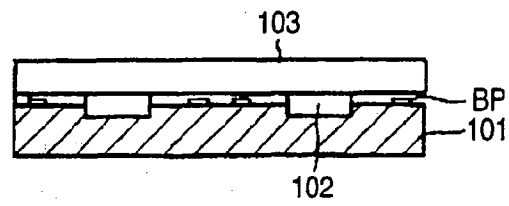


FIG. 22B

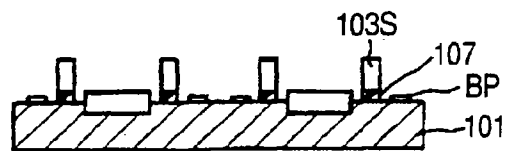


FIG. 22C

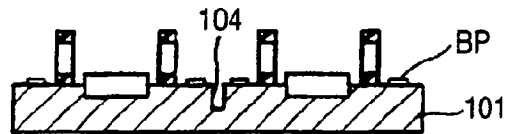


FIG. 23A

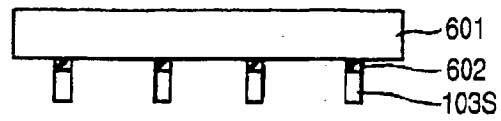


FIG. 23B

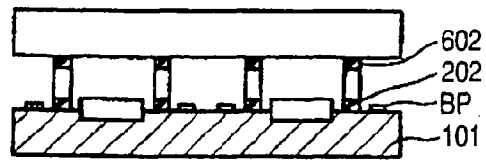


FIG. 23C

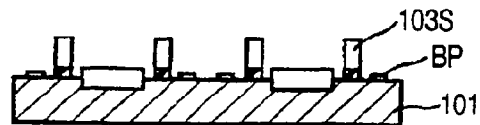


FIG. 23D

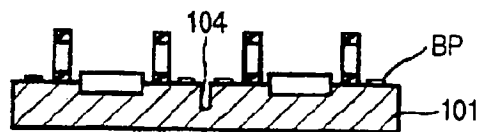


FIG. 24

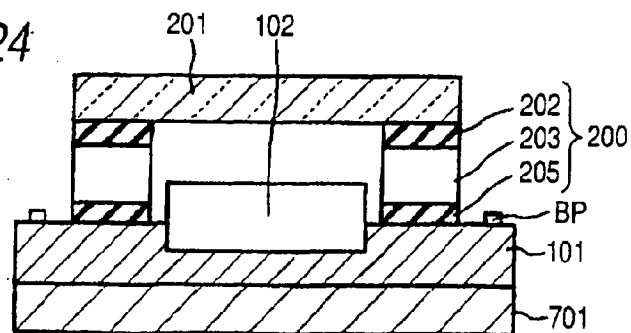


FIG. 25A

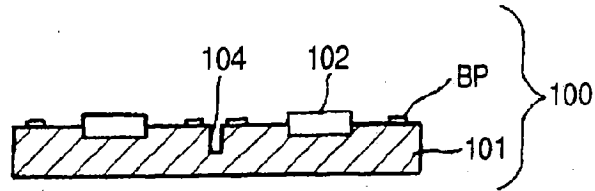


FIG. 25B

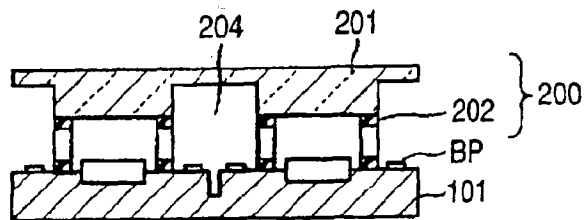


FIG. 25C

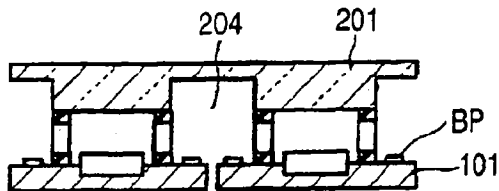


FIG. 25D

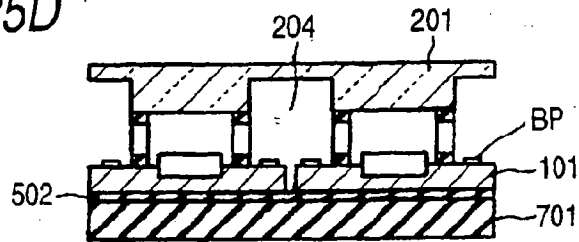


FIG. 25E

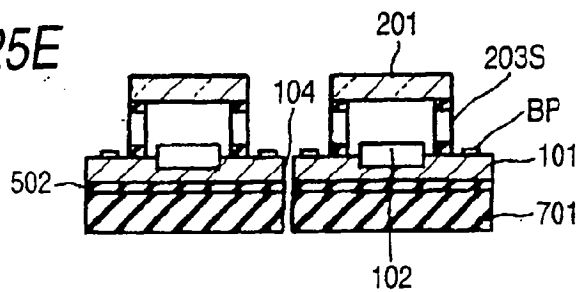


FIG. 26

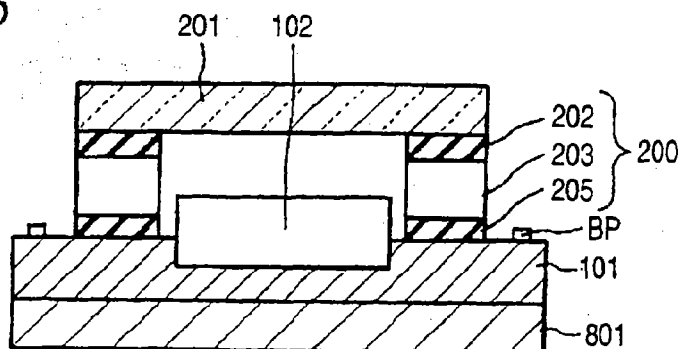


FIG. 27A

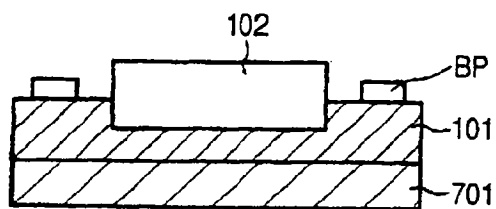


FIG. 27B

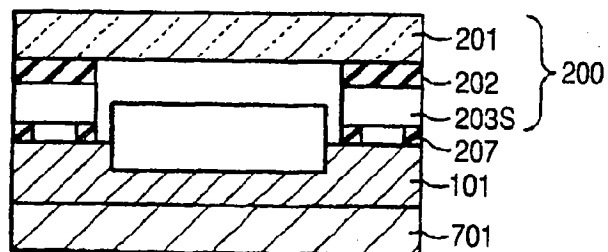


FIG. 27C

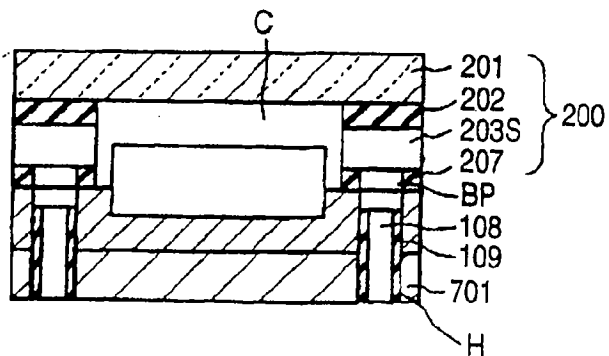


FIG. 28A

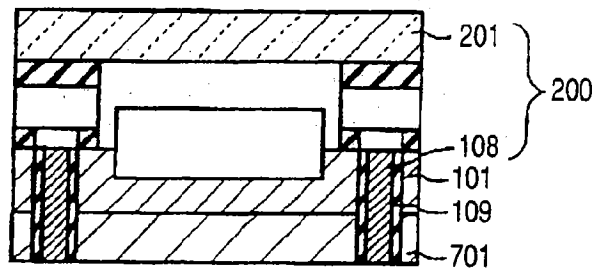


FIG. 28B

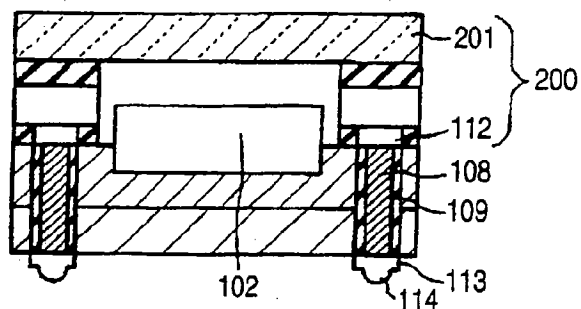


FIG. 28C

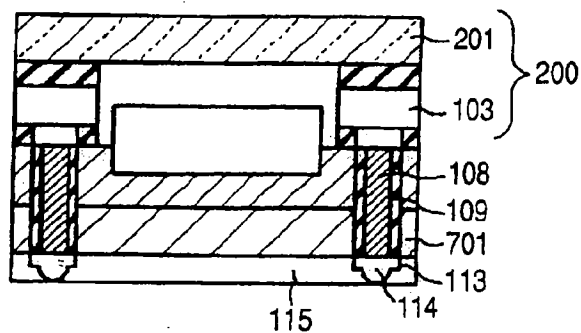


FIG. 28D

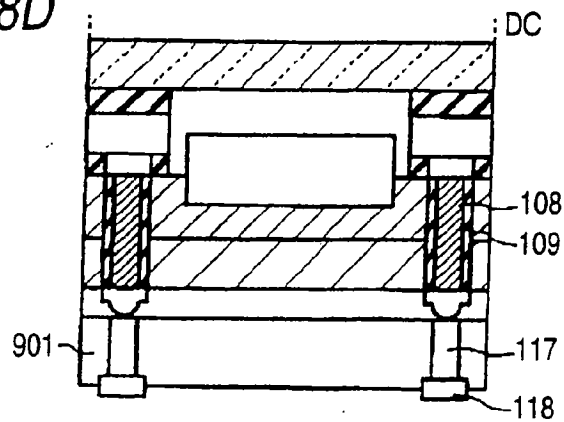


FIG. 29A

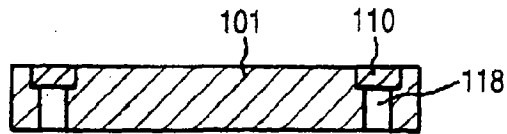


FIG. 29B

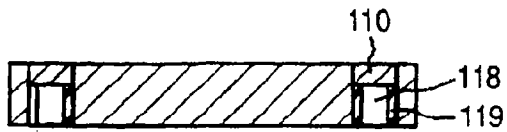


FIG. 29C

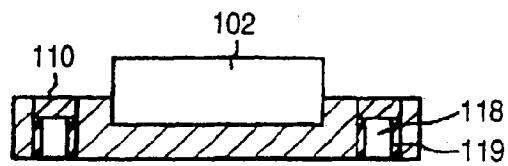


FIG. 29D

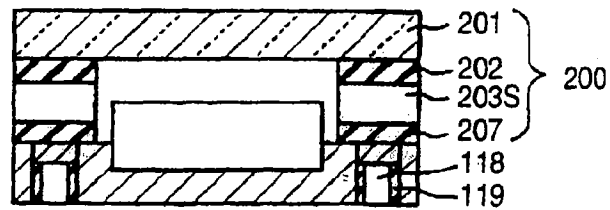


FIG. 29E

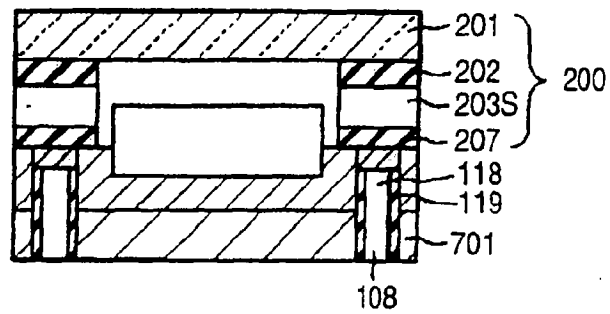


FIG. 30A

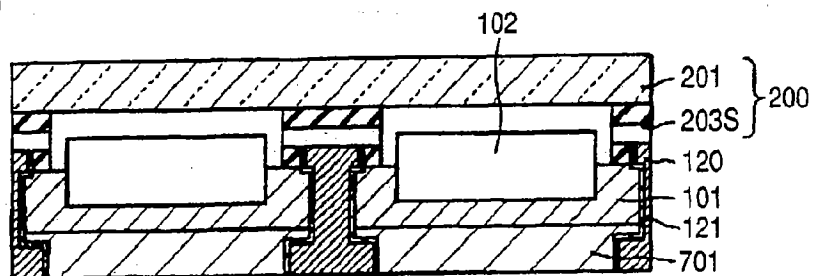


FIG. 30B

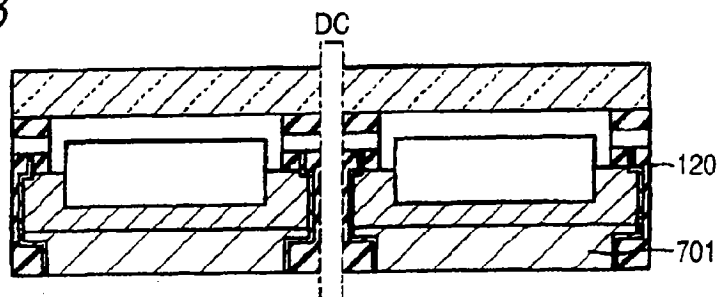


FIG. 31

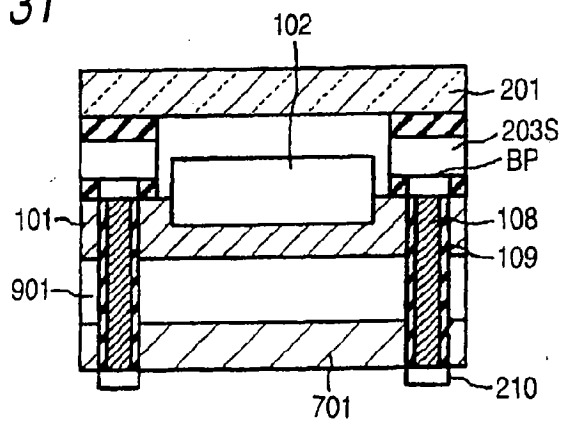


FIG. 32

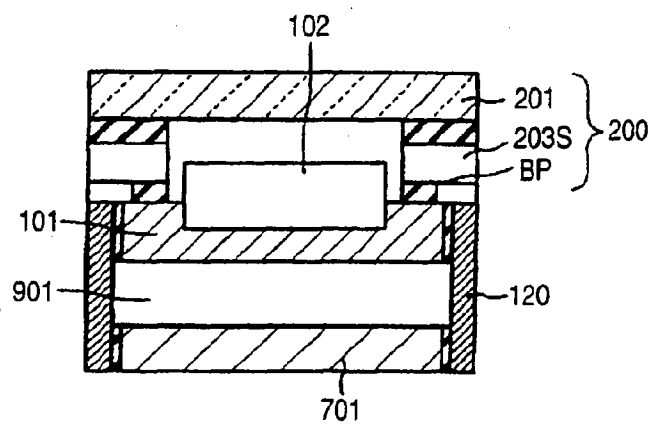


FIG. 33

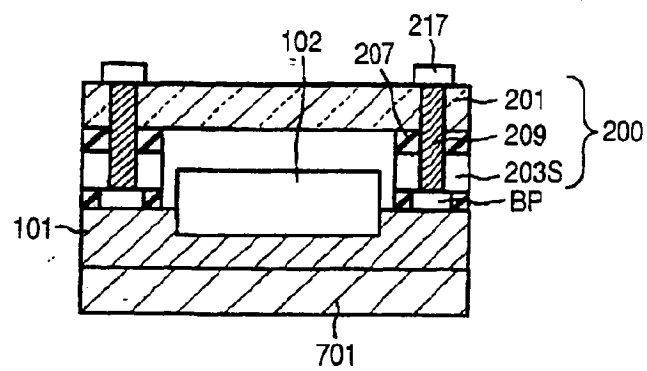


FIG. 34A

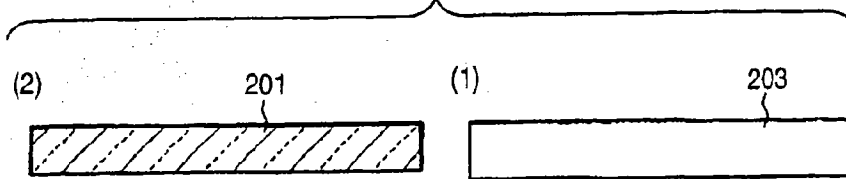


FIG. 34B



FIG. 34C

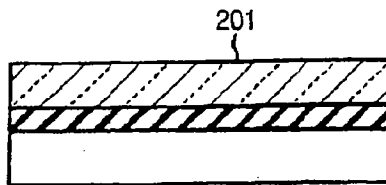


FIG. 34D

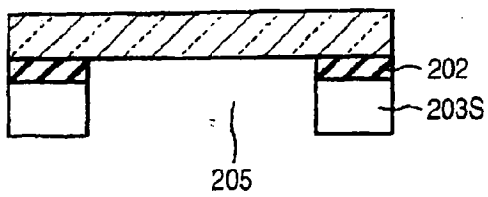


FIG. 34E

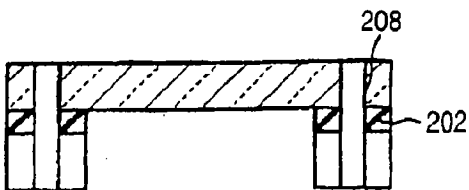


FIG. 35A

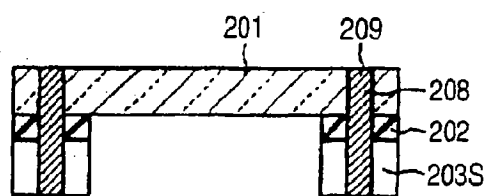


FIG. 35B

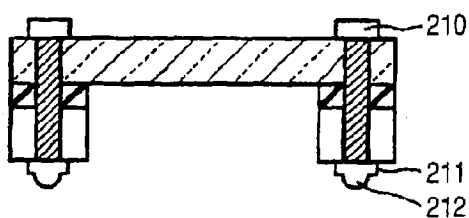


FIG. 35C

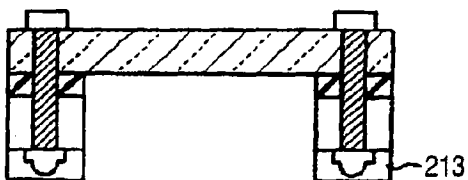


FIG. 35D

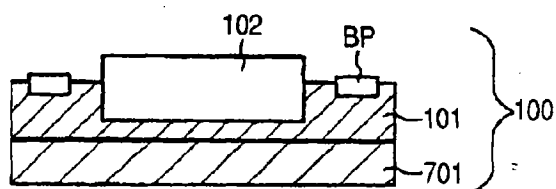


FIG. 35E

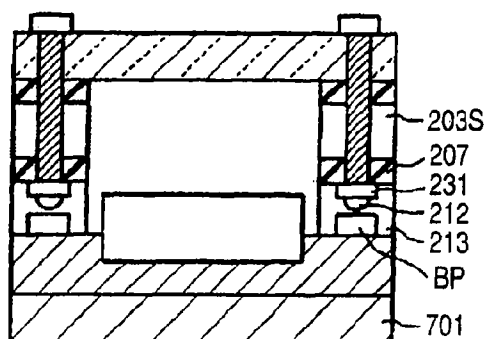


FIG. 36A

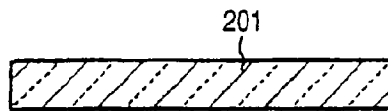


FIG. 36B

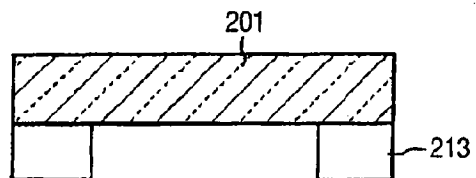


FIG. 36C

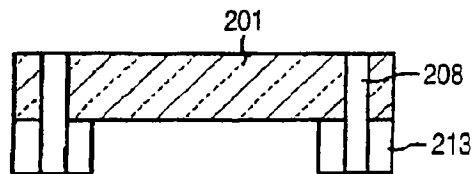


FIG. 37A

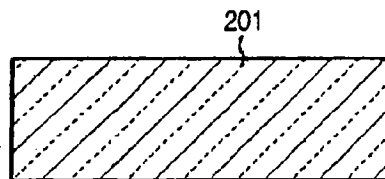


FIG. 37B

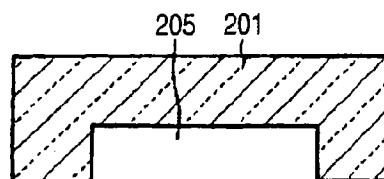


FIG. 37C

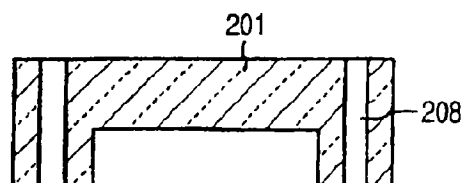


FIG. 38A

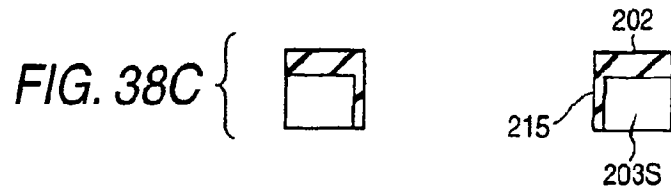
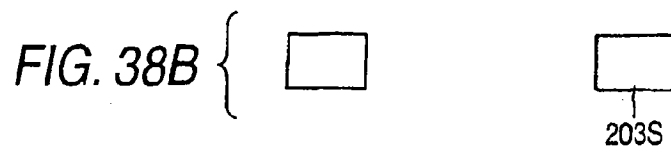
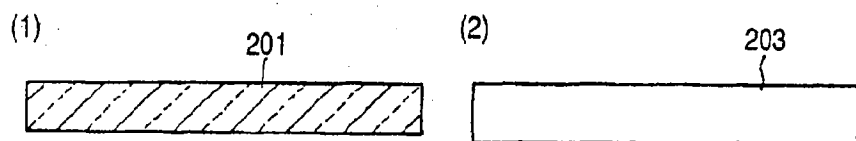


FIG. 38D

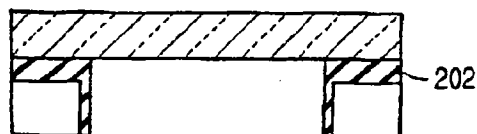


FIG. 38E

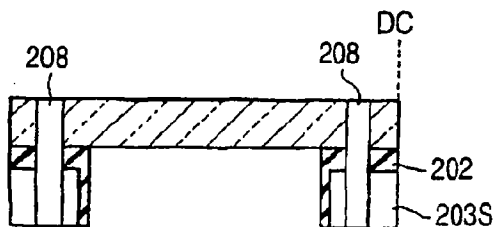


FIG. 39A

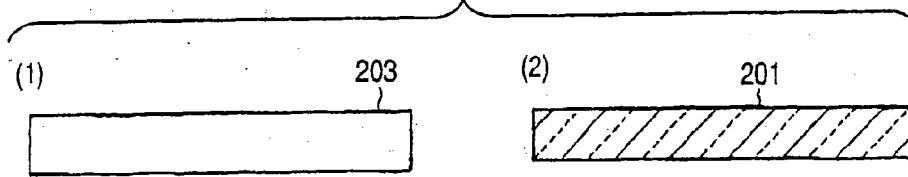


FIG. 39B

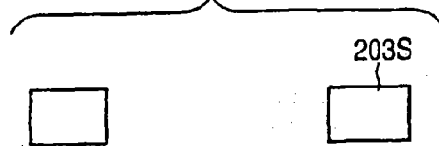


FIG. 39C

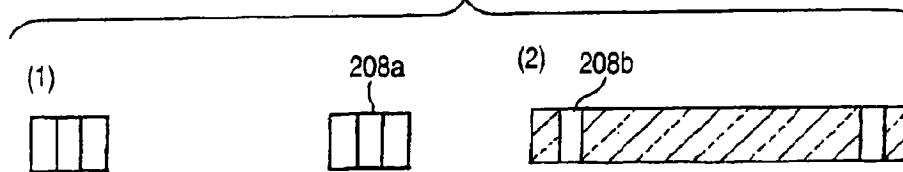


FIG. 39D

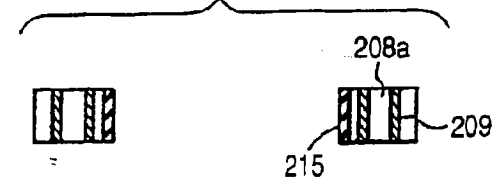


FIG. 39E

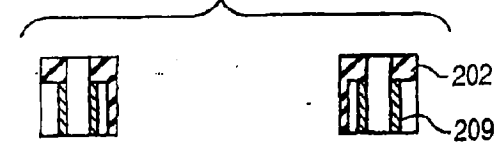


FIG. 39F

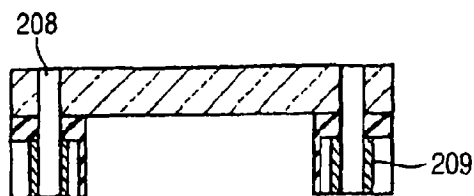


FIG. 40A

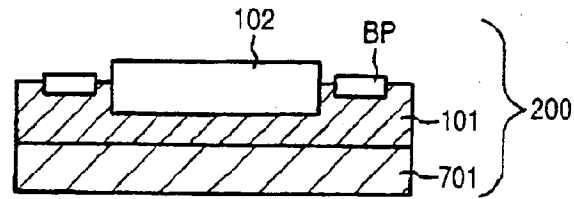


FIG. 40B

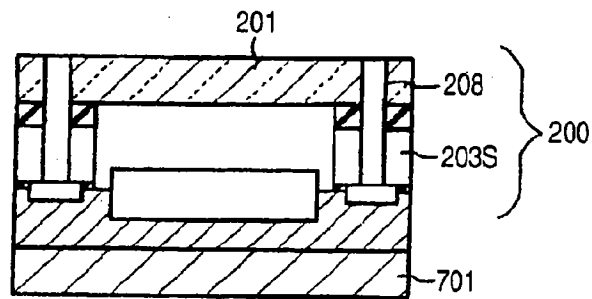


FIG. 40C

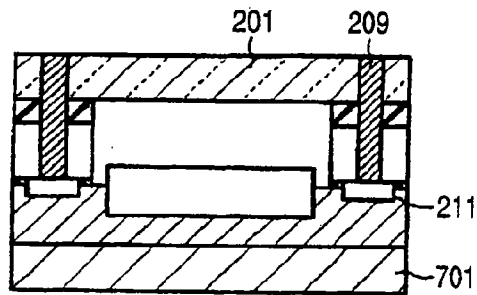


FIG. 40D

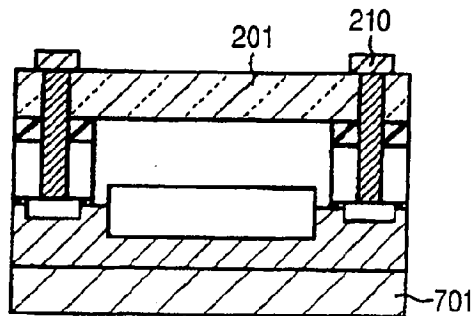


FIG. 41

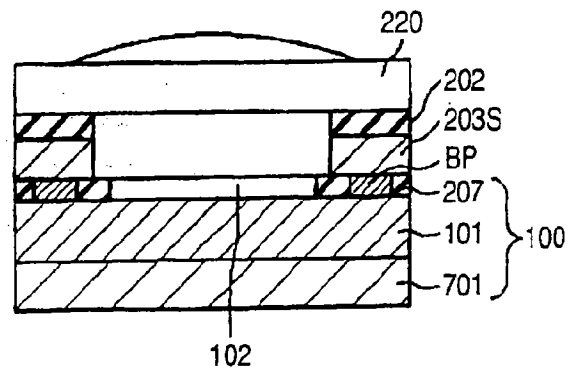


FIG. 42A

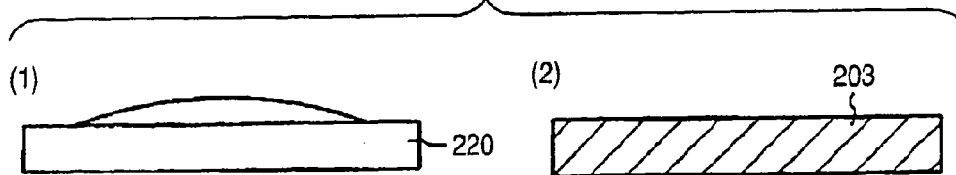


FIG. 42B

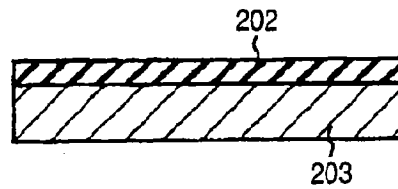


FIG. 42C

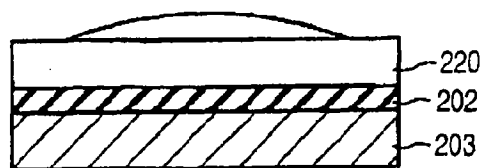


FIG. 42D

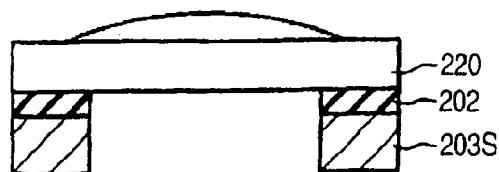


FIG. 43A

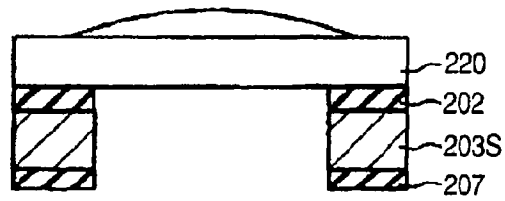


FIG. 43B

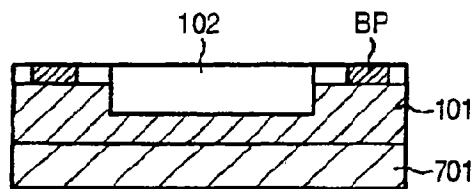


FIG. 43C

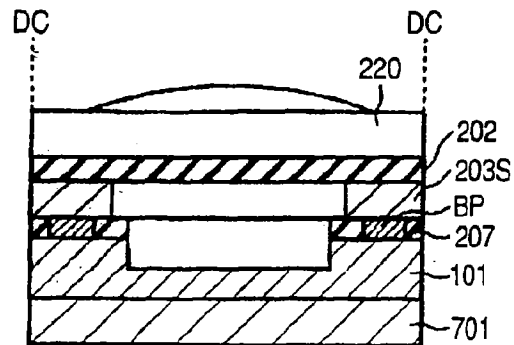


FIG. 44A

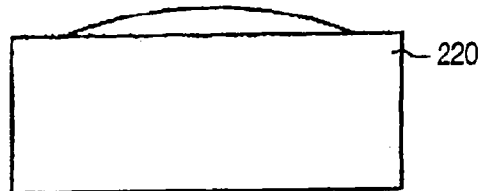


FIG. 44B

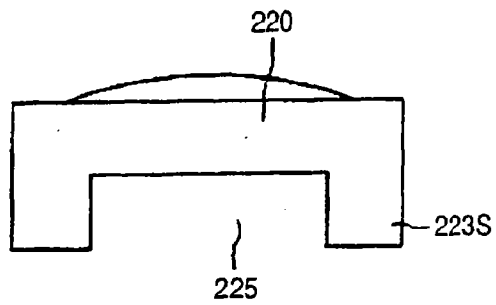


FIG. 45A

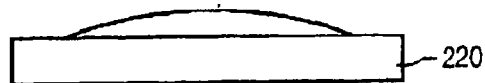


FIG. 45B

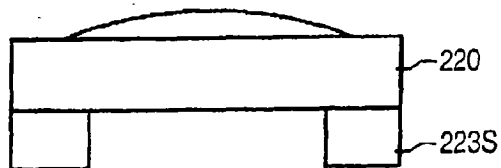


FIG. 46A

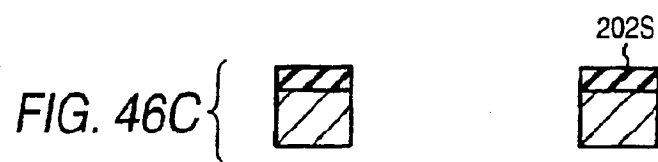
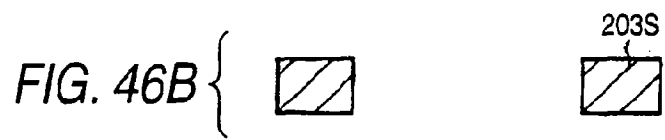
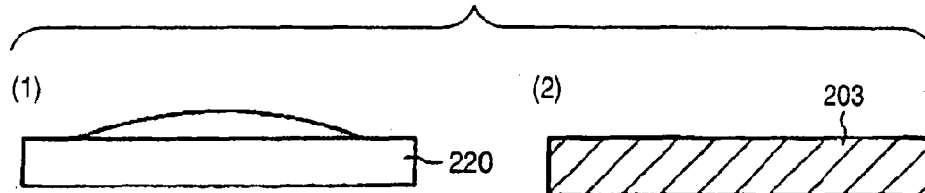


FIG. 46D



FIG. 47A

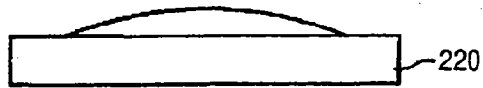


FIG. 47B



FIG. 47C

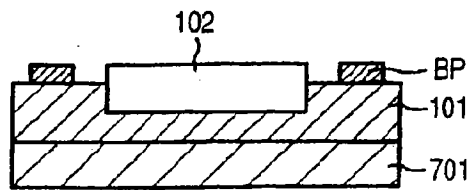


FIG. 47D

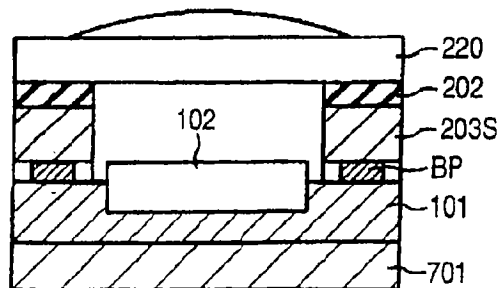


FIG. 48A

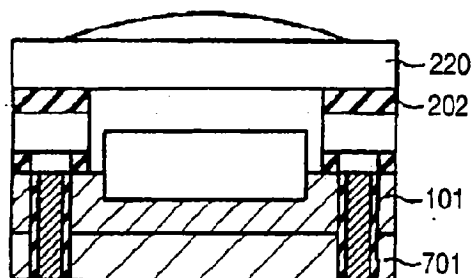


FIG. 48B

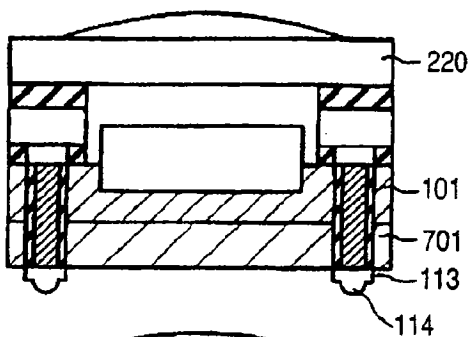


FIG. 48C

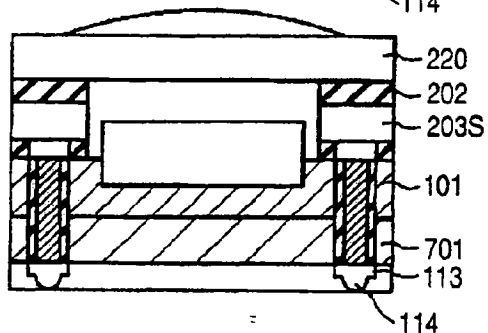


FIG. 48D

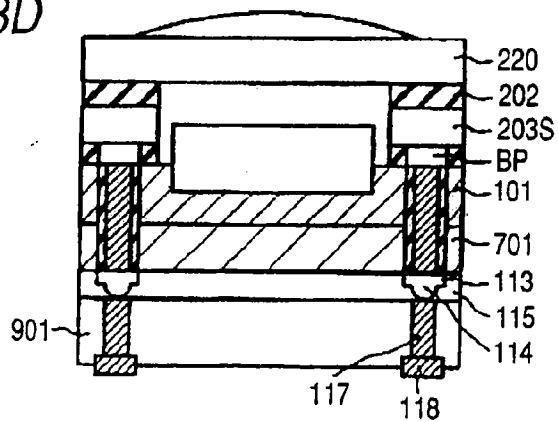


FIG. 49

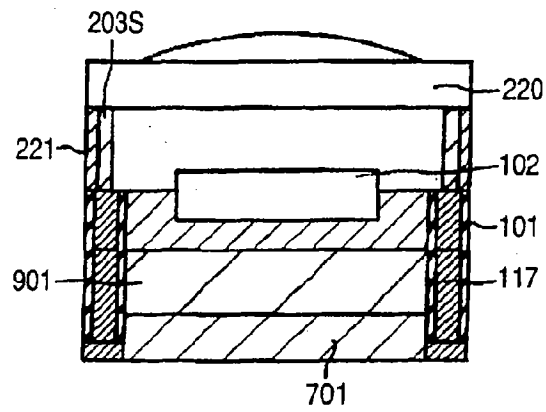


FIG. 50

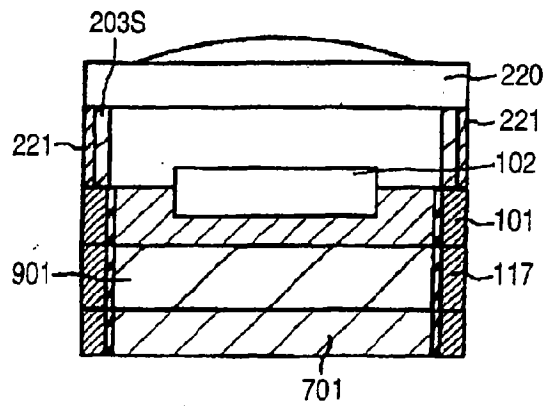


FIG. 51A



FIG. 51B



FIG. 51C



FIG. 51D



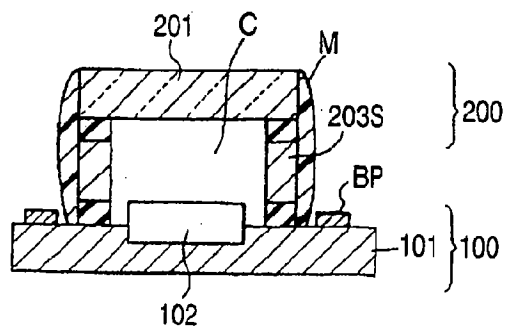
FIG. 51E

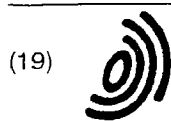


FIG. 51F



FIG. 52





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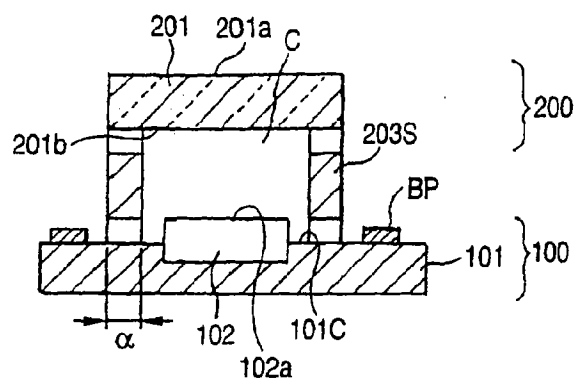
(54) **Solid-state imaging device and method for manufacturing the same**

(57) A solid-state imaging device, comprising: a semiconductor substrate (101) having a first surface; a solid-state imaging element (102) in the first surface of semiconductor substrate, the solid-state imaging element comprising a light-receiving region; a light-transmission member (201) having a second surface and a third surface, the second surface being opposite to the third surface, wherein the light-transmission member and the first

surface of the semiconductor substrate define a gap (C) between the second surface of the light-transmission member and an outer surface of the light-receiving region; and an external connection terminal (BP) connected to the solid-state imaging element, wherein the light-transmission member comprises low α -ray glass.

EP 1 503 420 A3

FIG. 1A





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EUROPEAN SEARCH REPORT

Application Number
EP 04 25 4637

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	EP 1 239 519 A (CANON KABUSHIKI KAISHA) 11 September 2002 (2002-09-11) * paragraphs [0045], [0063], [0075], [0156], [0164]; figures 1a,9b,11,26b,35 *	1,5-8, 10,12,13	INV. H01L27/146
P,X, L	EP 1 387 397 A (FUJI PHOTO FILM CO., LTD) 4 February 2004 (2004-02-04) * paragraphs [0092], [0103], [0107], [0112], [0114], [0127] - [0140]; figures 1-3 *	1-13	
E	EP 1 463 120 A (FUJI PHOTO FILM CO., LTD) 29 September 2004 (2004-09-29) * paragraphs [0028] - [0030], [0033], [0047]; figures 2,10-14 *	1-13	
			TECHNICAL FIELDS SEARCHED (IPC)
			H01L
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 6 June 2006	Examiner Cabrita, A
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document	

EPC FORM 1503 03.02 (P2-001)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 04 25 4637

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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06-06-2006

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 1239519	A	11-09-2002	CN 1377181 A	30-10-2002
			CN 1633162 A	29-06-2005
			TW 536833 B	11-06-2003
			US 2004012698 A1	22-01-2004

EP 1387397	A	04-02-2004	CN 1489218 A	14-04-2004

EP 1463120	A	29-09-2004	CN 1542931 A	03-11-2004
			JP 2004312666 A	04-11-2004
			US 2006038204 A1	23-02-2006
			US 2004189855 A1	30-09-2004

EPO FORM P0489

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82